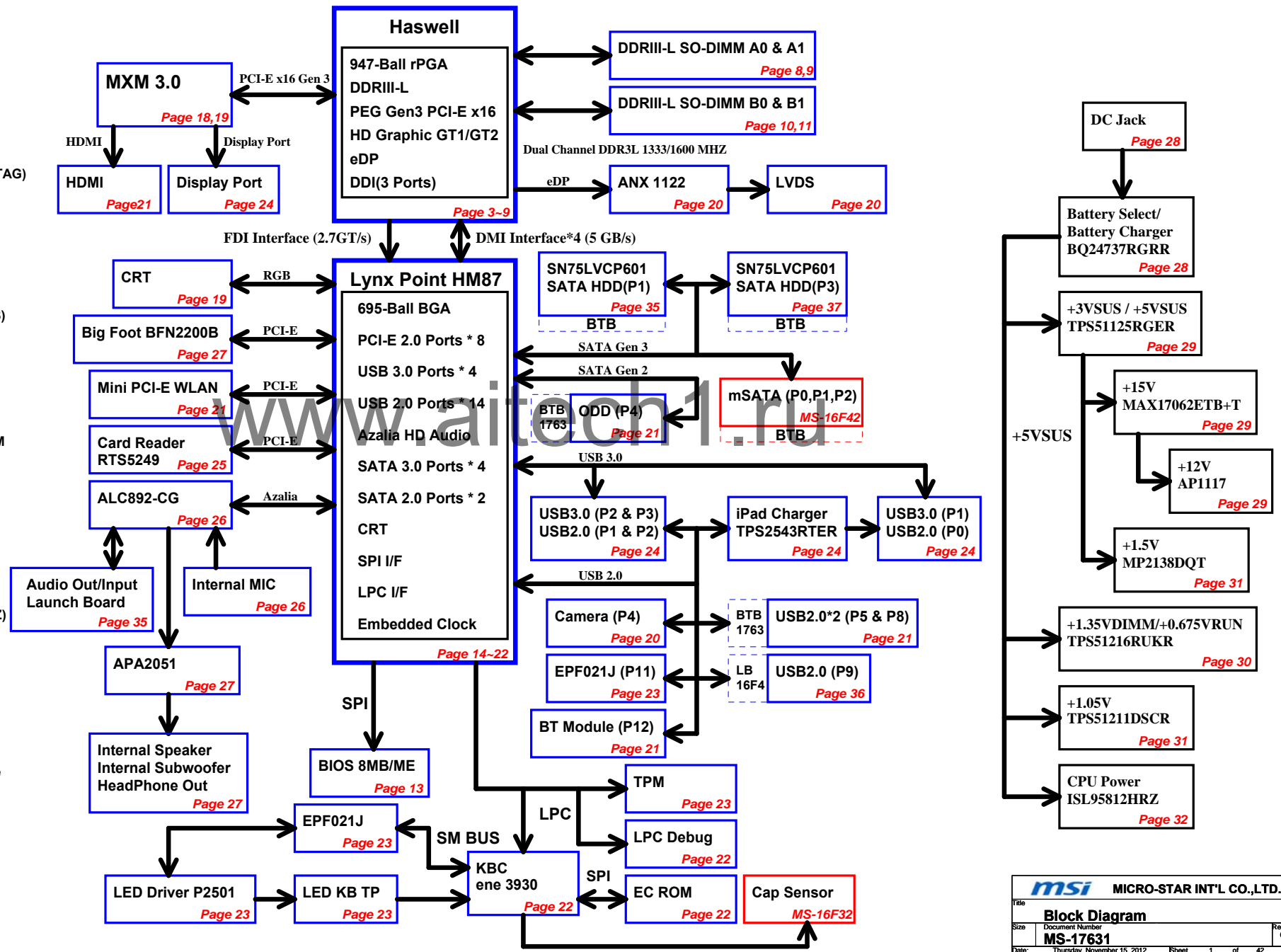


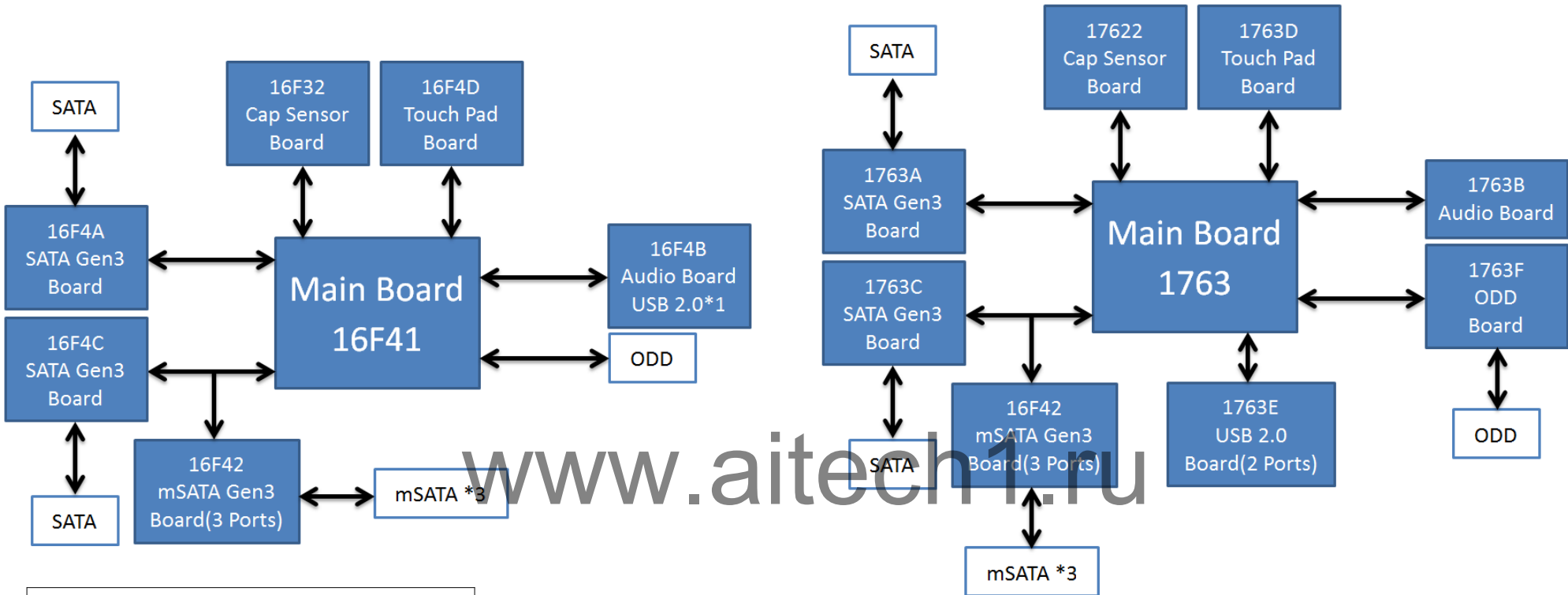
Shark Bay Platform

MS-1763 Ver.0A 2012/10/24

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 Page 03:History
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 Page 28:Battery Select/Charger
 Page 29:System Power
 Page 30:+1.35VDIMM/+0.675VRUN
 Page 31:+1.05VRUN/+1.5VRUN
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 Page 35:1763B_IO/Audio Board
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 Page 39:1763F_ODD Board
 Page 40:Impedance/Clock Distribution
 Page 41:Power on Sequence
 Page 42:Power Down & MXM Sequence
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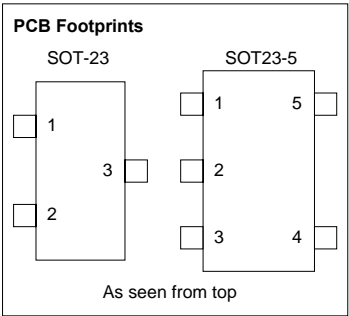
Board Diagram



Voltage Rails			
Power Plane	Voltage	Active In	Description
PWR_SRC	19V or 12 V	S0, S3-S5	Power Source
+5VALW	5V	S0, S3-S5	
+3VALW	3.3V	S0, S3-S5	
+5VSUS	5V	S0, S3	
+3VSUS	3.3V	S0, S3	
+1_35VDIMM	1.35V	S0, S3	DDR3L Power
+5VRUN	5V	S0	
+3VRUN	3.3V	S0	
+1_5VRUN	1.5V	S0	PCH Power for I/O
+12V_FAN	12V	S0	Fan Power
+15V	15V	S0	LED Keyboard Power
+0_675VRUN	0.675V	S0	
+1_05VRUN	1.05V	S0	
+VCC_CORE	1.2V	S0	Processor Core Power Rail

Net Naming Conventions
Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

Power States						
	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*SUS	+V*RUN
S0 (Full on)	High	High	High	On	On	On
S3 (Suspend to RAM)	Low	High	High	On	On	Off
S4 (Suspend to Disk)	Low	Low	High	On	Off	Off
S5 (Soft off)	Low	Low	Low	On	Off	Off

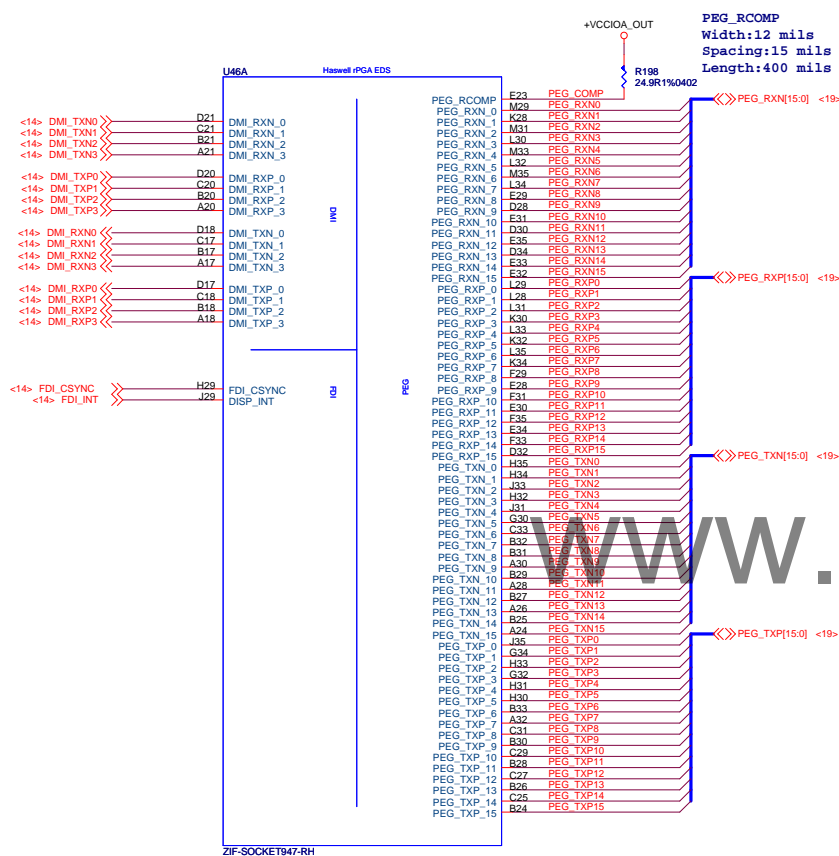
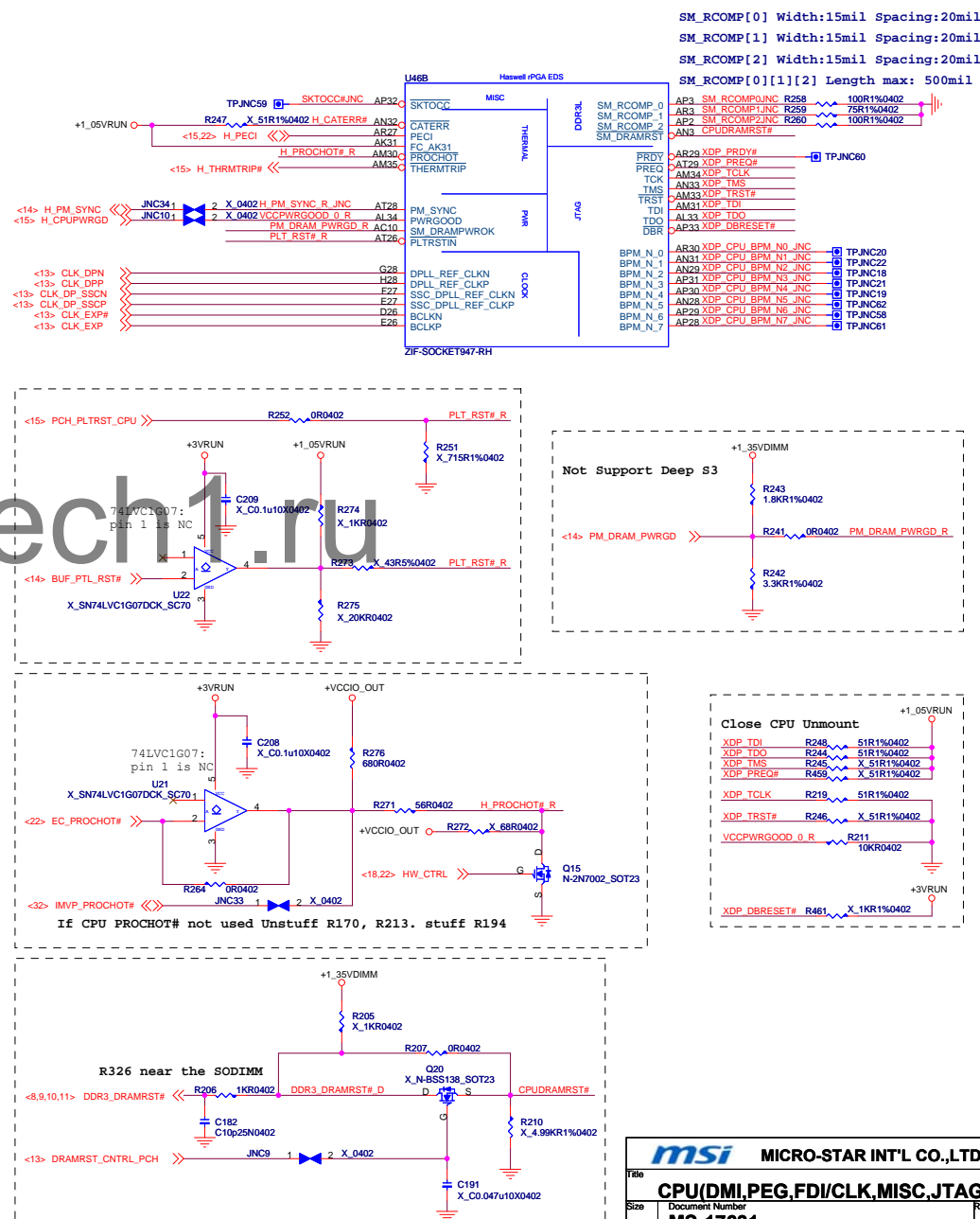


MS-17631 Change List

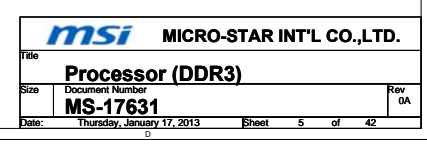
Date	Page	Description	Date	Page	Description	Date	Page	Description
2012.11.20	14	R335 Unstuff						
	20	Change U30 SDA & SCL Pin						
	25	CardReader Change to RTS 5249						
2013.01.14	18	Modify MXM 5VRUN Power						
	19	Modify MXM GC6						
	20	Modify ANX 1122 SMB Channel						
		Ver. Change to 1.0						
2013.01.21	28	PQ13 & PQ14 Change to D03-0444703-A68						

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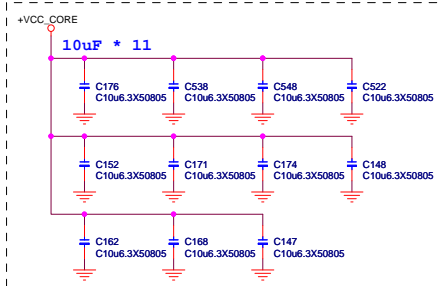
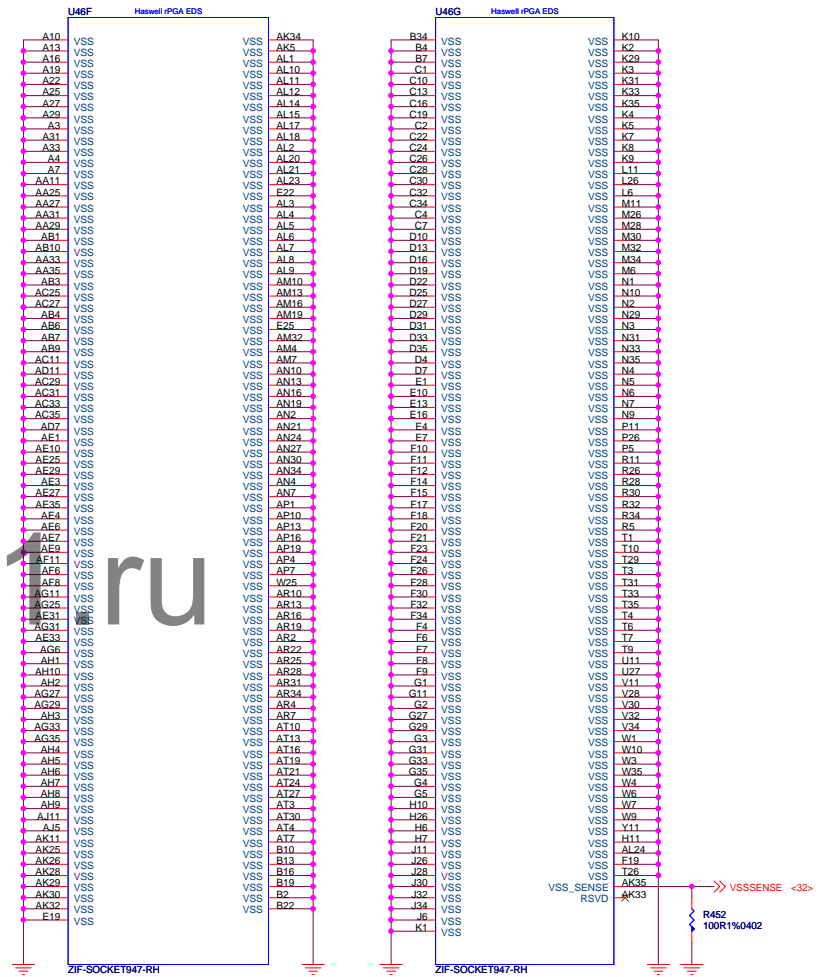
Haswell Processor (DMI,PEG,FDI)

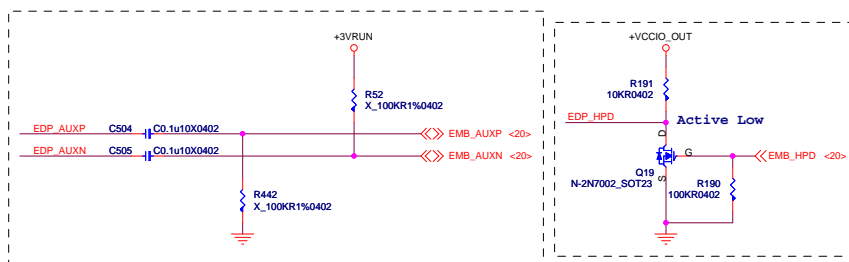
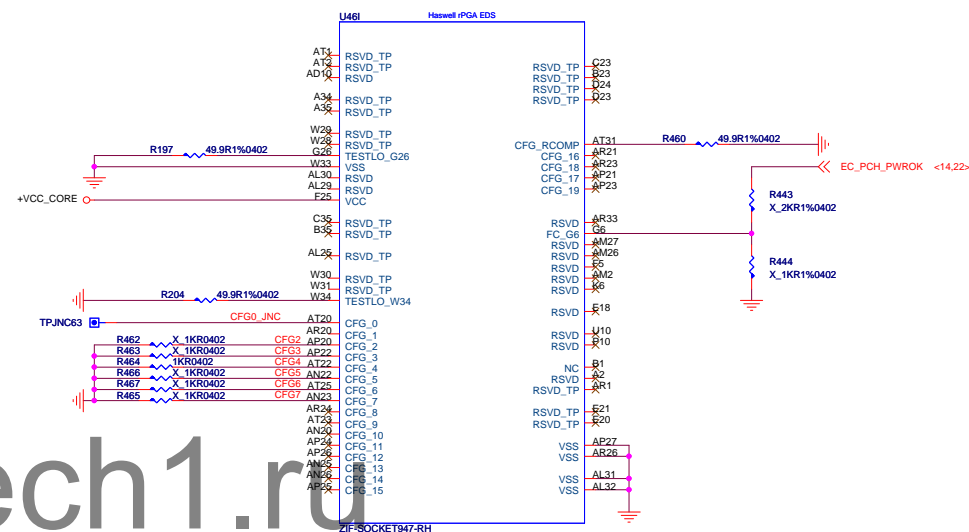
**Haswell Processor (CLK,MISC,JTAG)**

SA_MA_3	AC5	M_A_A4	M_B_D034	L4	SB_D0_33
SA_MA_4	AC4	M_A_A5	M_B_D035	M4	SB_D0_34
SA_MA_5	AD6	M_A_A6	M_B_D036	L1	SB_D0_35
SA_MA_6	AC3	M_A_A7	M_B_D037	M1	SB_D0_36
SA_MA_7	AD5	M_A_A8	M_B_D038	L5	SB_D0_37
SA_MA_8	AC2	M_A_A9	M_B_D039	M5	SB_D0_38
SA_MA_9	AD7	M_A_A10	M_B_D040	G7	SB_D0_39
SA_MA_10	AD1	M_A_A11	M_B_D041	J8	SB_D0_40
SA_MA_11	AD4	M_A_A12	M_B_D042	G8	SB_D0_41
SA_MA_12	AD3	M_A_A13	M_B_D043	G9	SB_D0_42



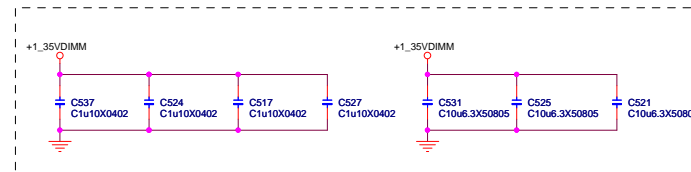
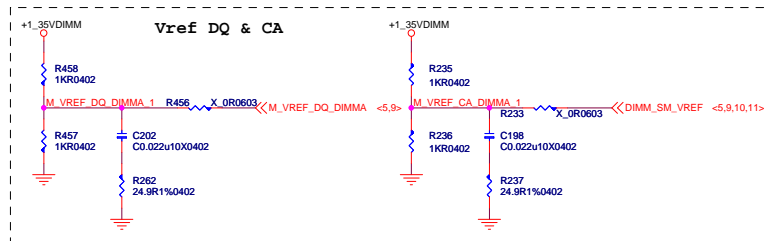
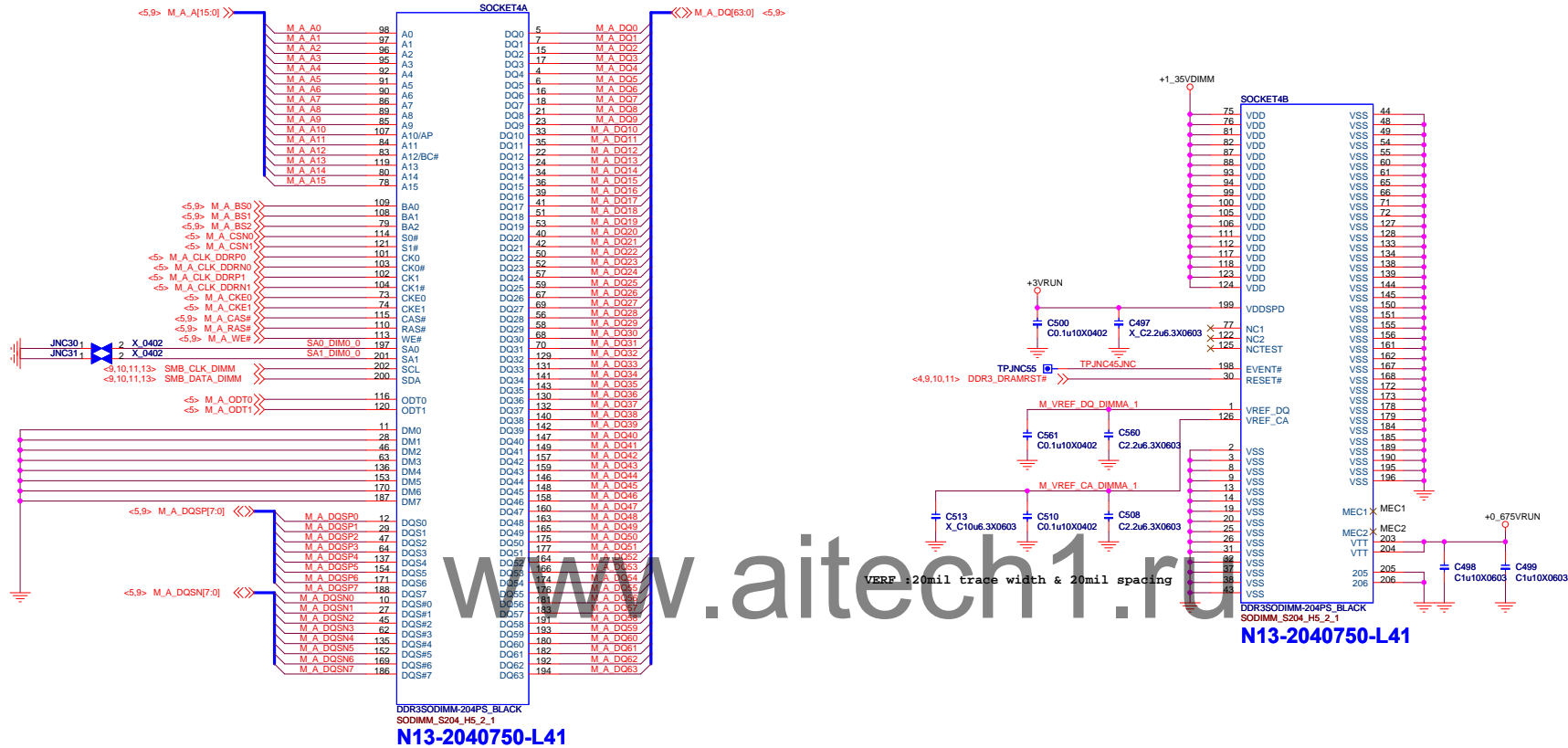
Haswell Processor (Gnd)



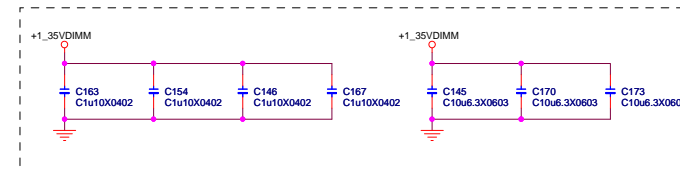
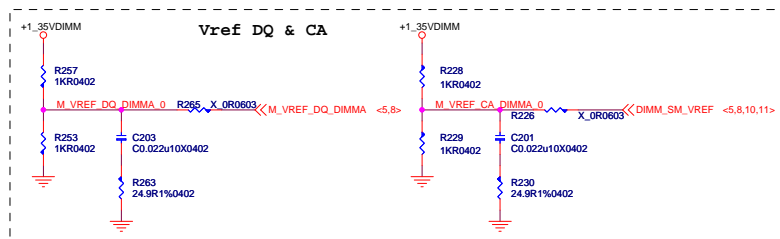
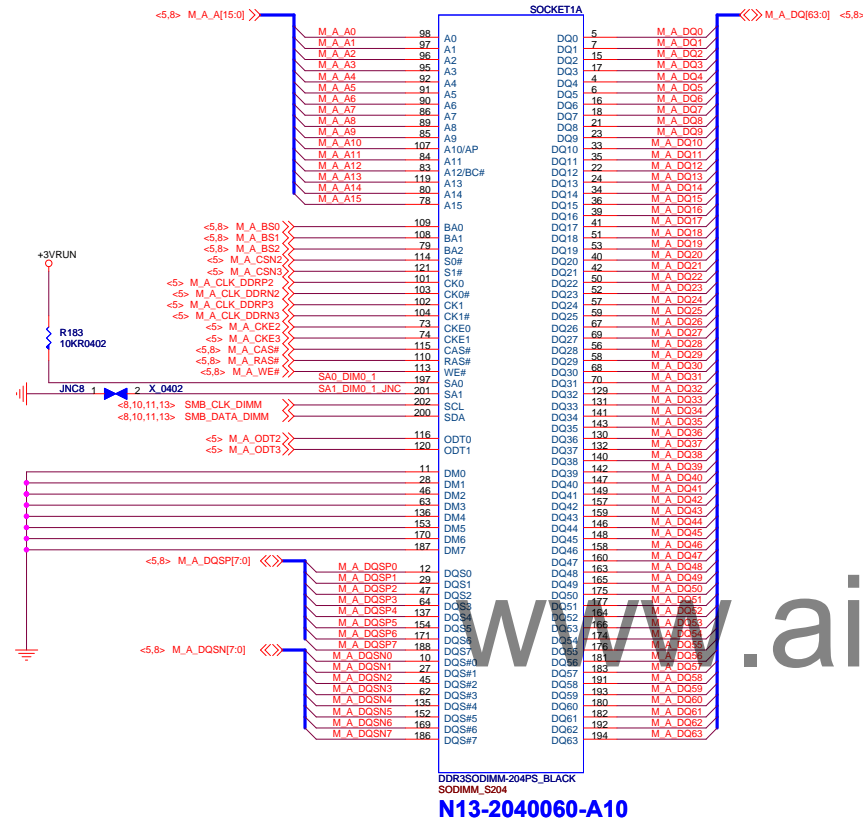
Haswell Processor (Reserved)

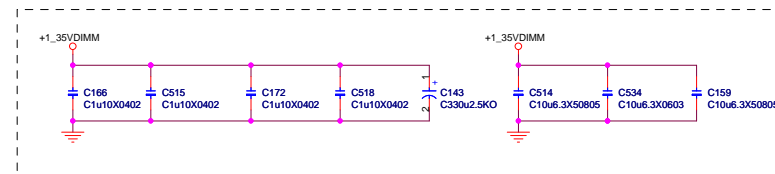
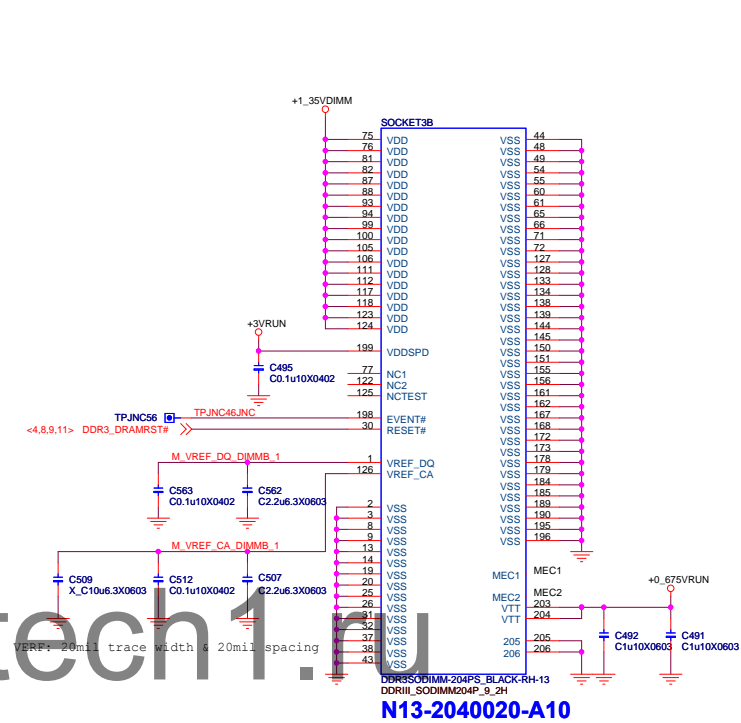
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

SODIMM #A0

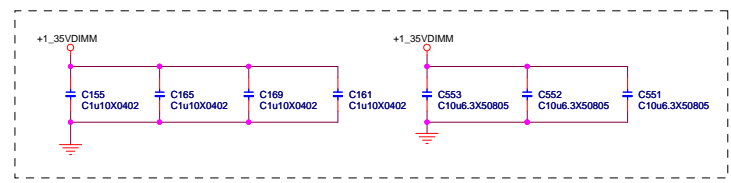
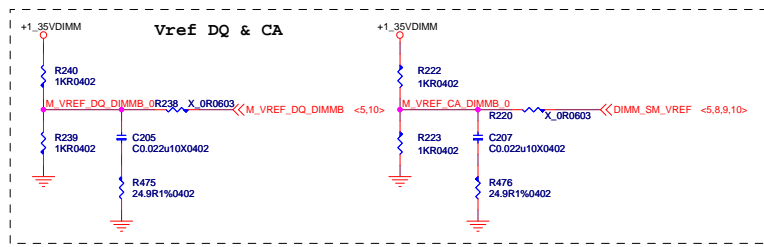
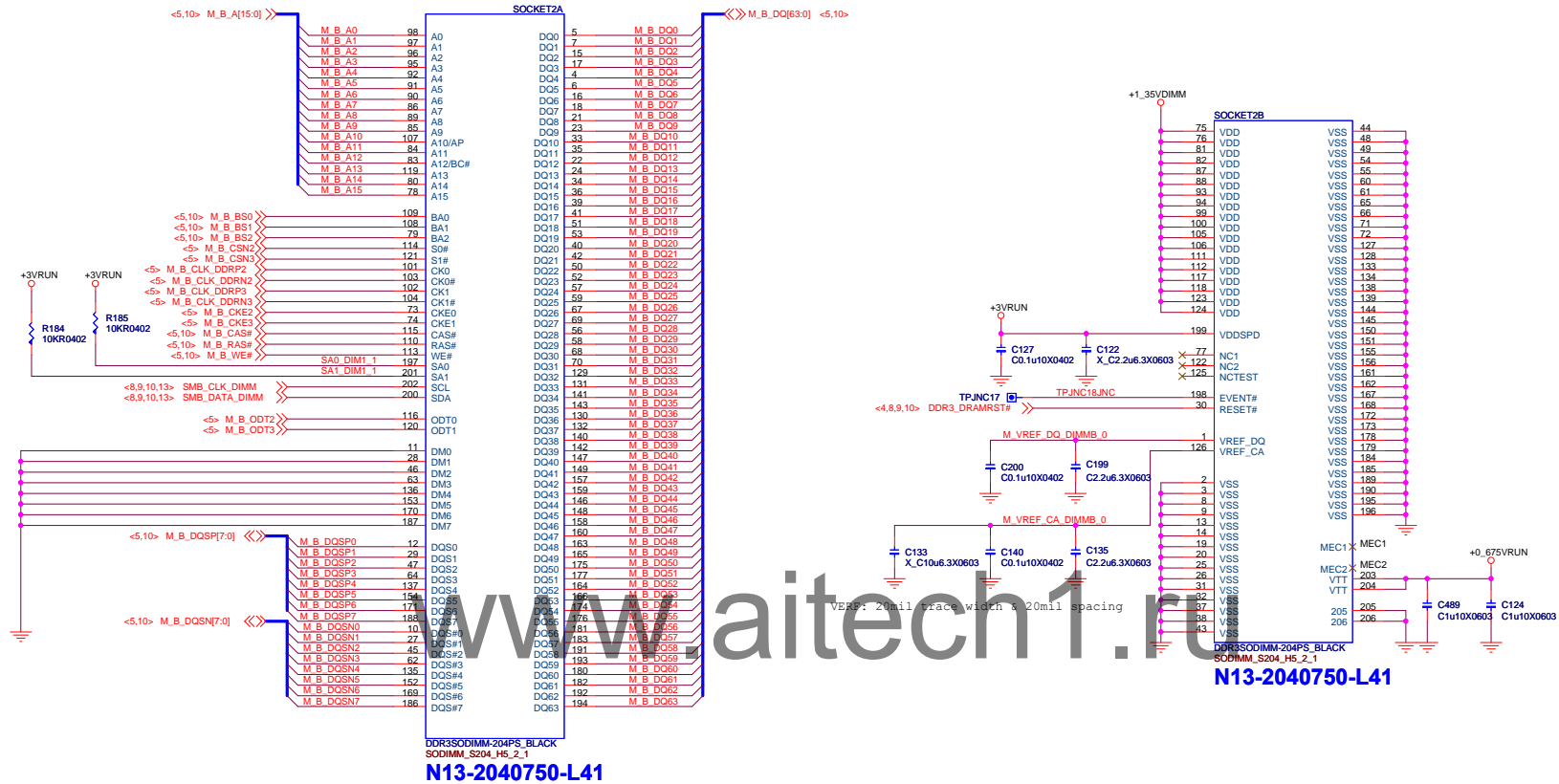


SODIMM #A1

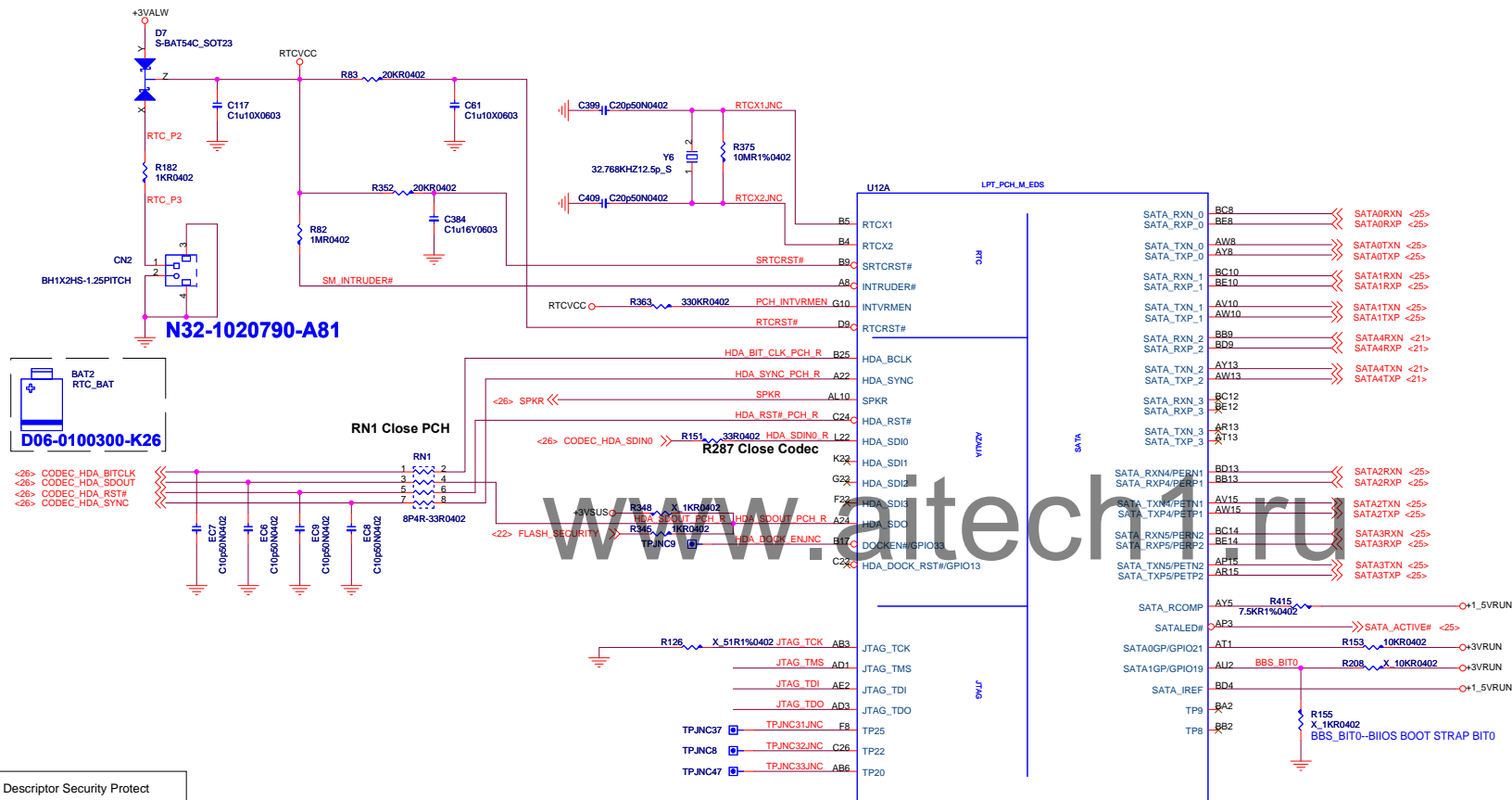


[illegible]

SODIMM #B1



Lynx Point (HDA,JTAG,SATA)



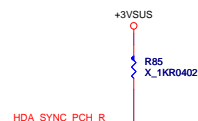
SATA	
Port	Device
0	mSATA Gen3(6Gb/s)
1	mSATA Gen3(6Gb/s)
2	ODD(Gen2)
3	NC
4	mSATA Gen3(6Gb/s)
5	To A board(Gen3)

Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

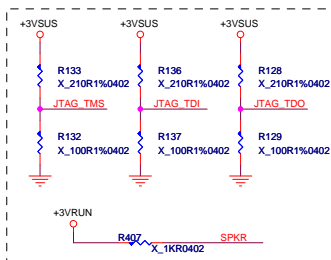
Signal has a weak internal pull-down
Note: The weak internal pull-down is disabled after PLTRST# deasserts.

SPK	<p>The Signal has a weak internal pull-down</p> <p>Note: the internal pull-down is disabled after PLTRST# deasserts.</p> <p>If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)</p>
-----	--

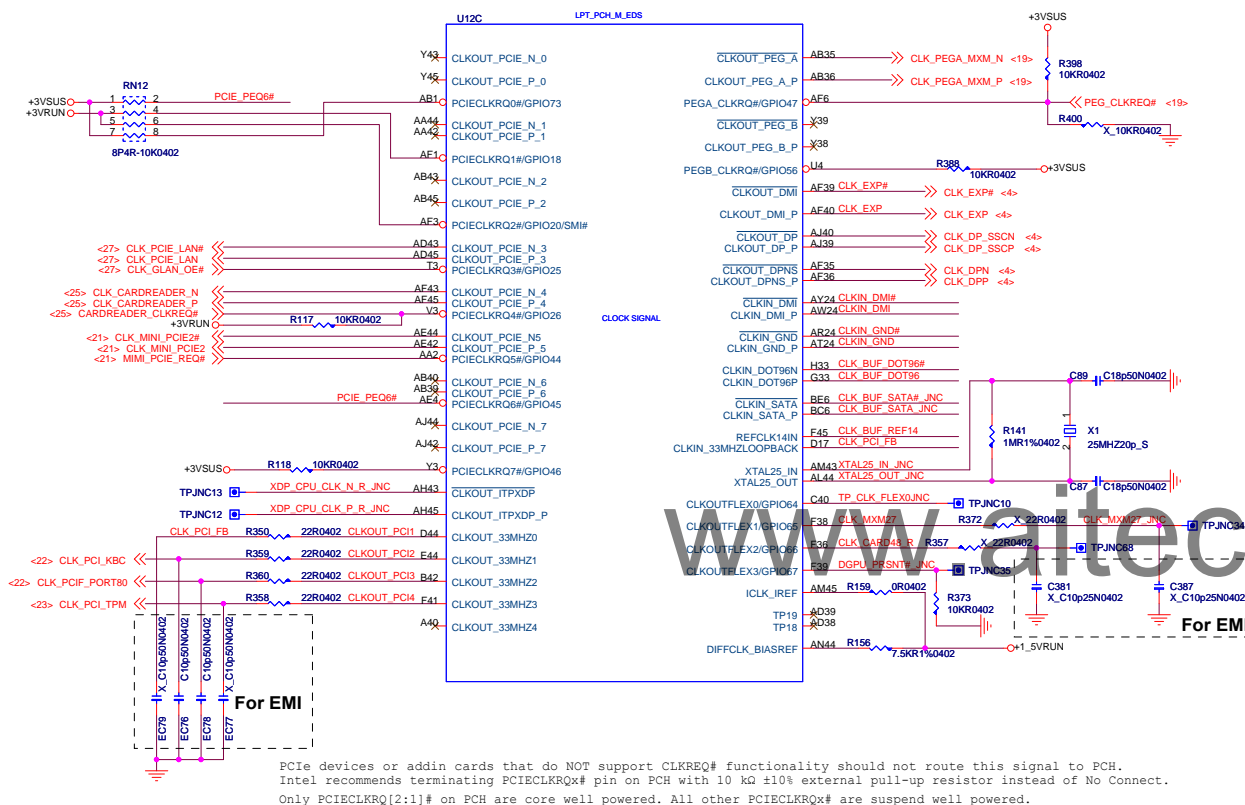
Reserved for Codec use RUN.



HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the V_{Imin} at PCH input. Therefore, platform may need to isolate this signal from the codec during the strap phase. The following example circuits maybe used to achieve this purpose.



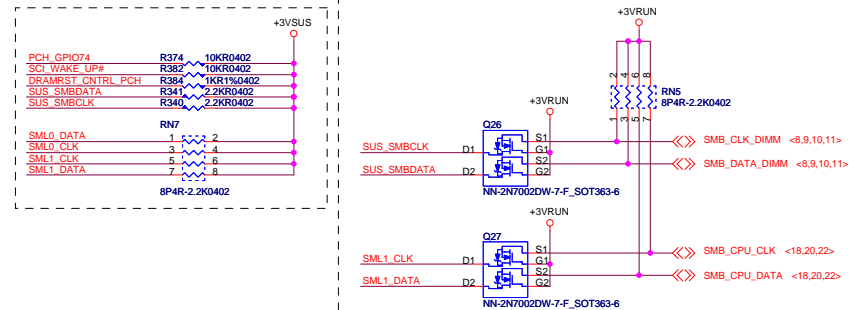
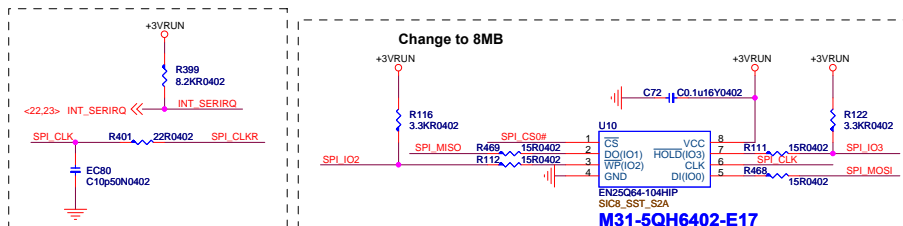
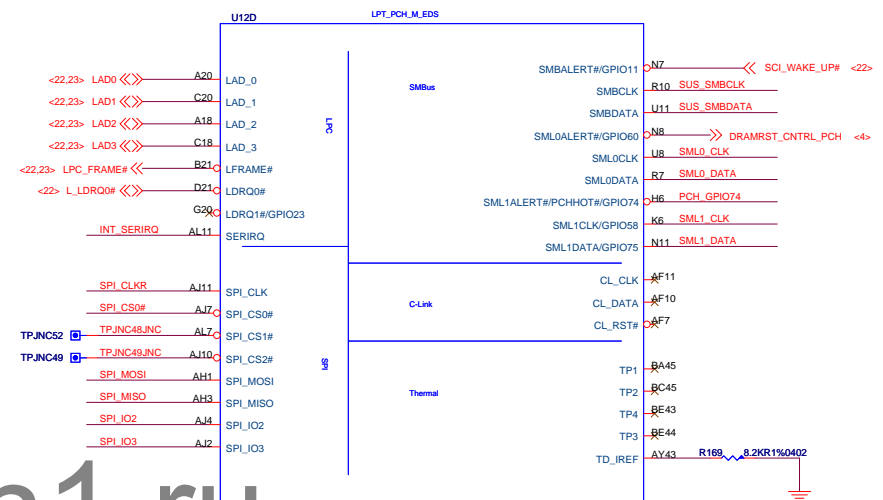
Lynx Point (Clock)



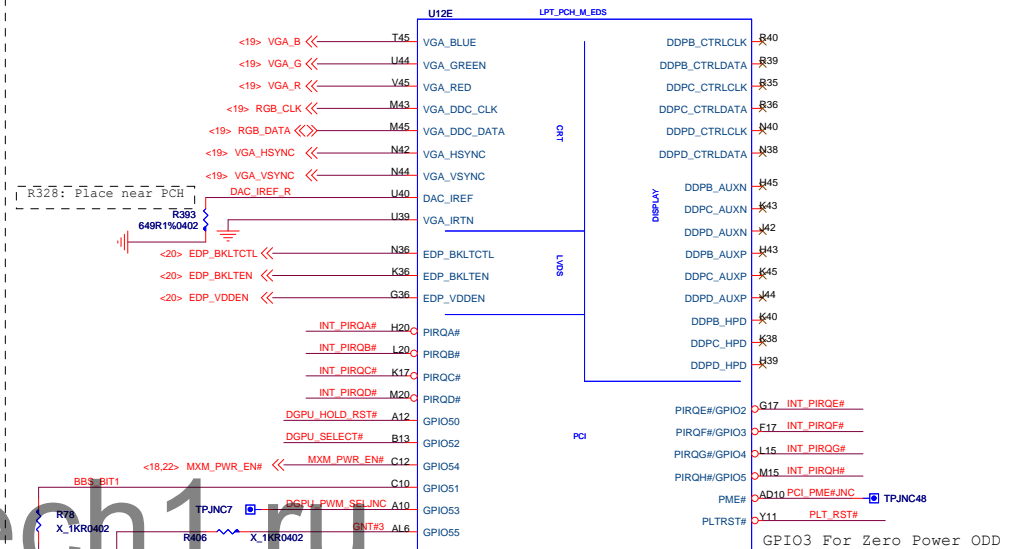
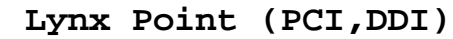
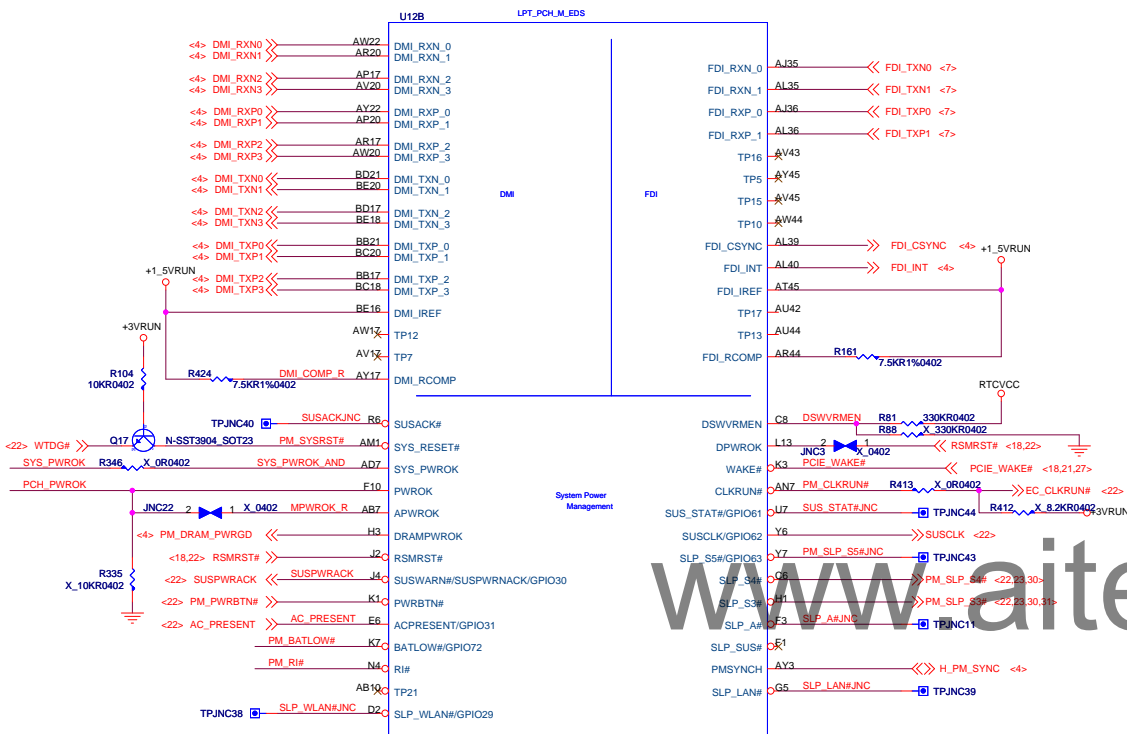
*Disable PCIE OBFF(BIOS)

For Integrated Clock Generation Mode

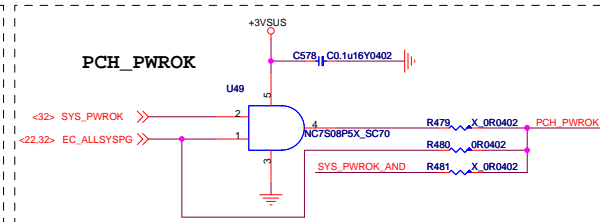
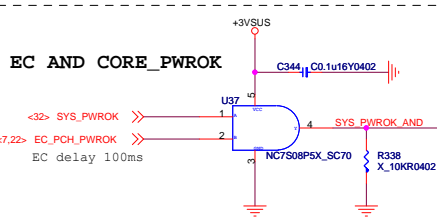
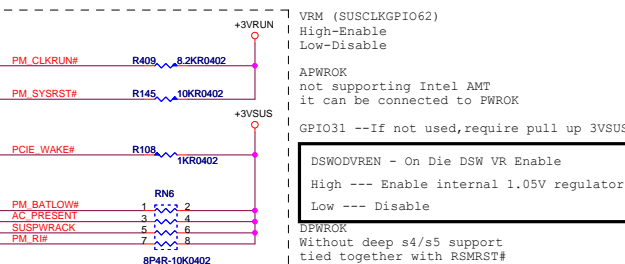
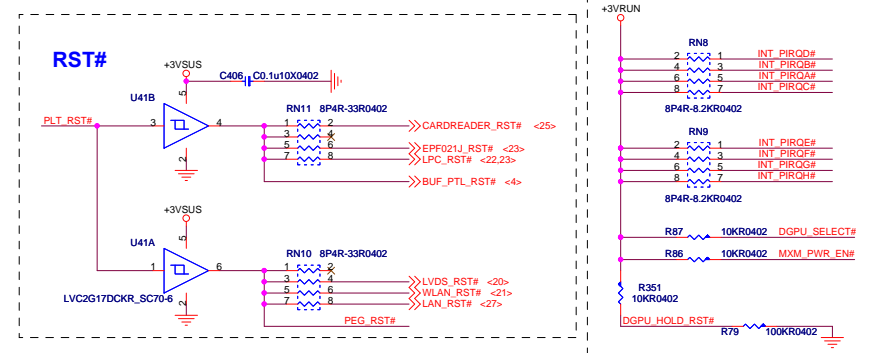
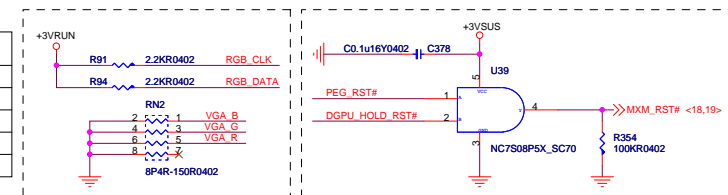
Lynx Point (LPC, SMBUS)



Lynx Point (DMI, FDI)

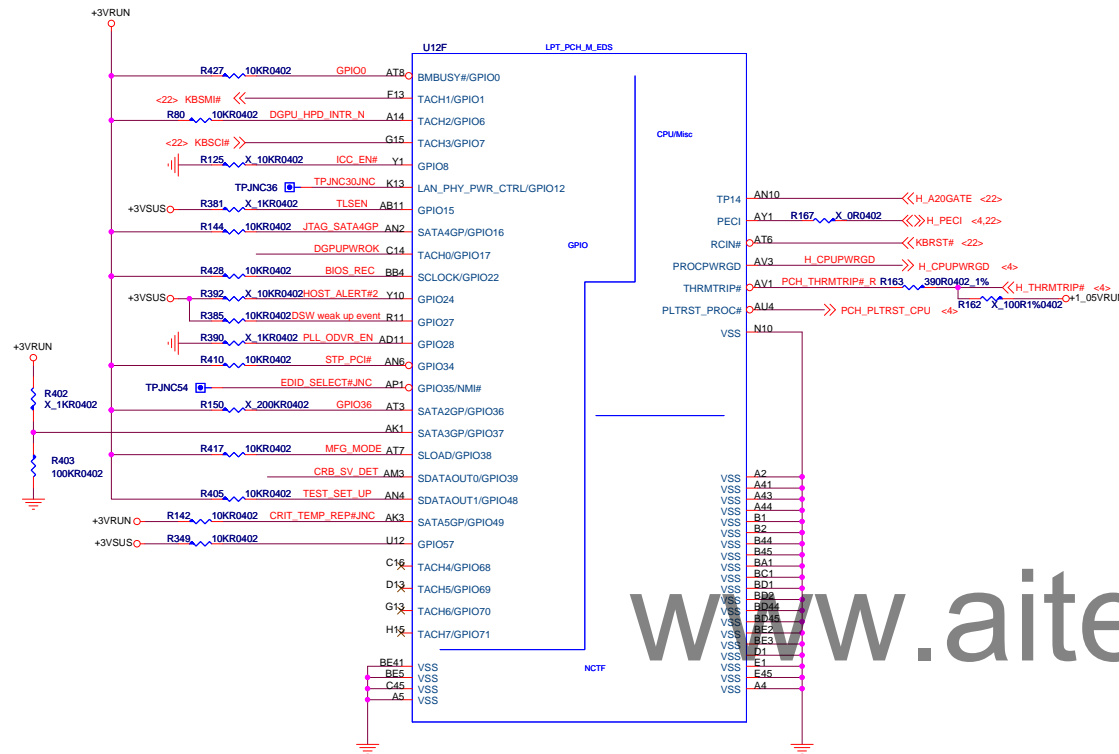


BIOS BOOT STRAP BIT		
BBS_BIT0	BBS_BIT1	BOOT BIOS LOCATION
0	0	LPC
0	1	RESERVED(NAND)
1	0	N/A
1	1	SPI

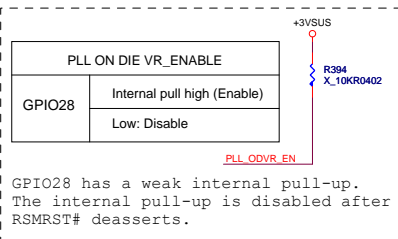


Lynx Point (GPIO,MISC)

Lynx Point (Gnd)

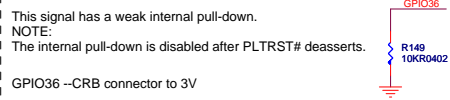


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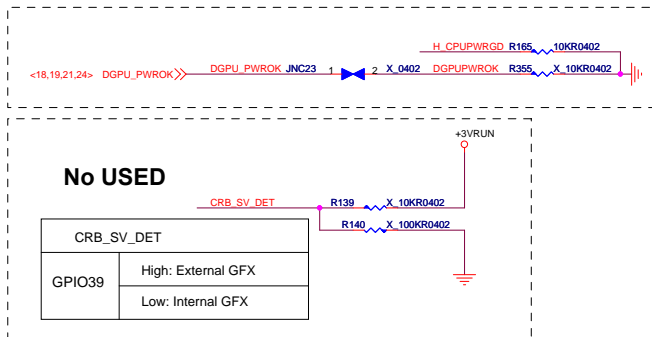
GPIO28 has a weak internal pull-up.
The internal pull-up is disabled after RSMRST# deasserts.

SATA3GP/GPIO37
This signal has a weak internal pull-down.
NOTE:
The internal pull-down is disabled after PLTRST# deasserts.
NOTE:
This signal should not be pulled high when strap is sampled.



This signal has a weak internal pull-down.
NOTE:
The internal pull-down is disabled after PLTRST# deasserts.

GPIO36 --CRB connector to 3V

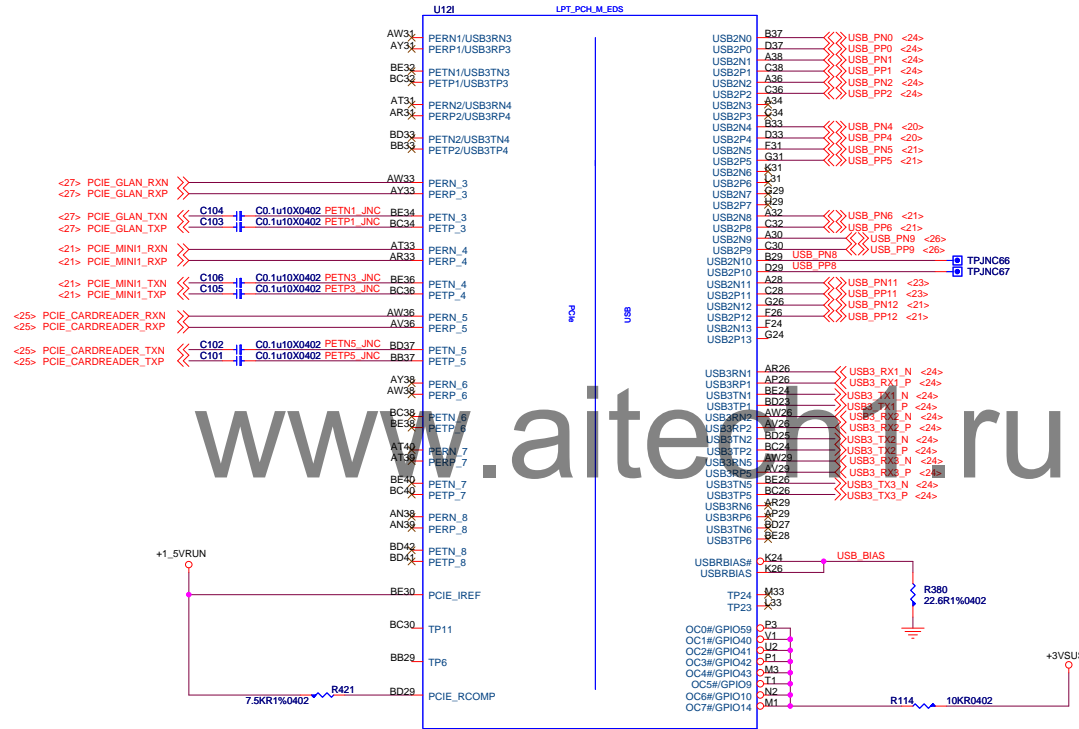


GPIO0 & 6 & 16 & 17 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN
GPIO57 --If not used,require pull up 3VSUS
GPIO15--Not support AMT,Transport Layer Security Disable(High is support TLS,internal pull-down)
GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin
GPIO35 --Define to EDID Select (If not used,require pull down)

SATA2GP/GPIO36 (net name: FDI_OVRVLTG) & SATA3GP/GPIO37 (net name: SATA_ODD_PRSTNT#)
Sampled at Rising edge of PWROK.
Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

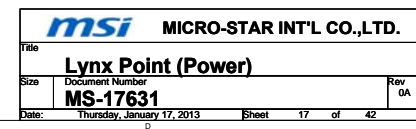
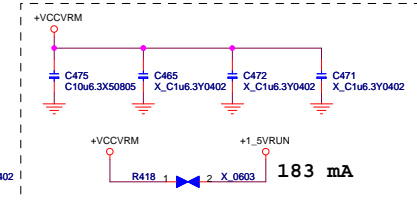
Lynx Point (PCIE,USB)

PCI-E	
Port	Device
3	Giga Lan
4	Mini PCIE-WLAN
5	Card Reader

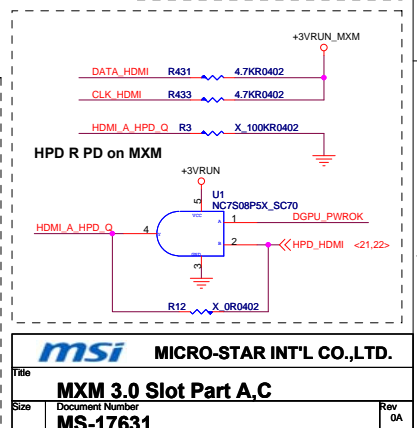
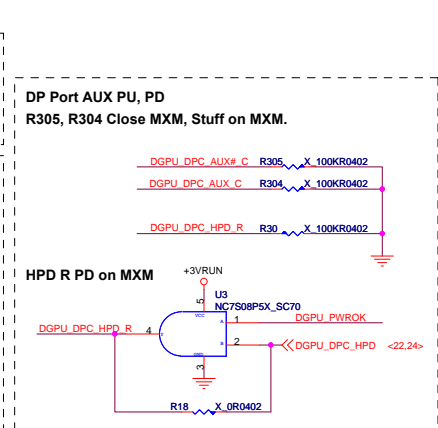
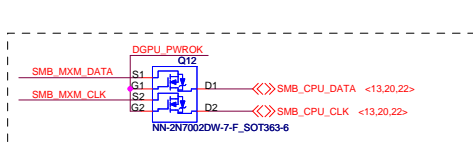
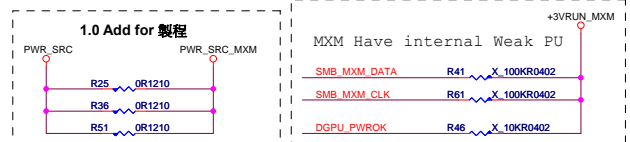
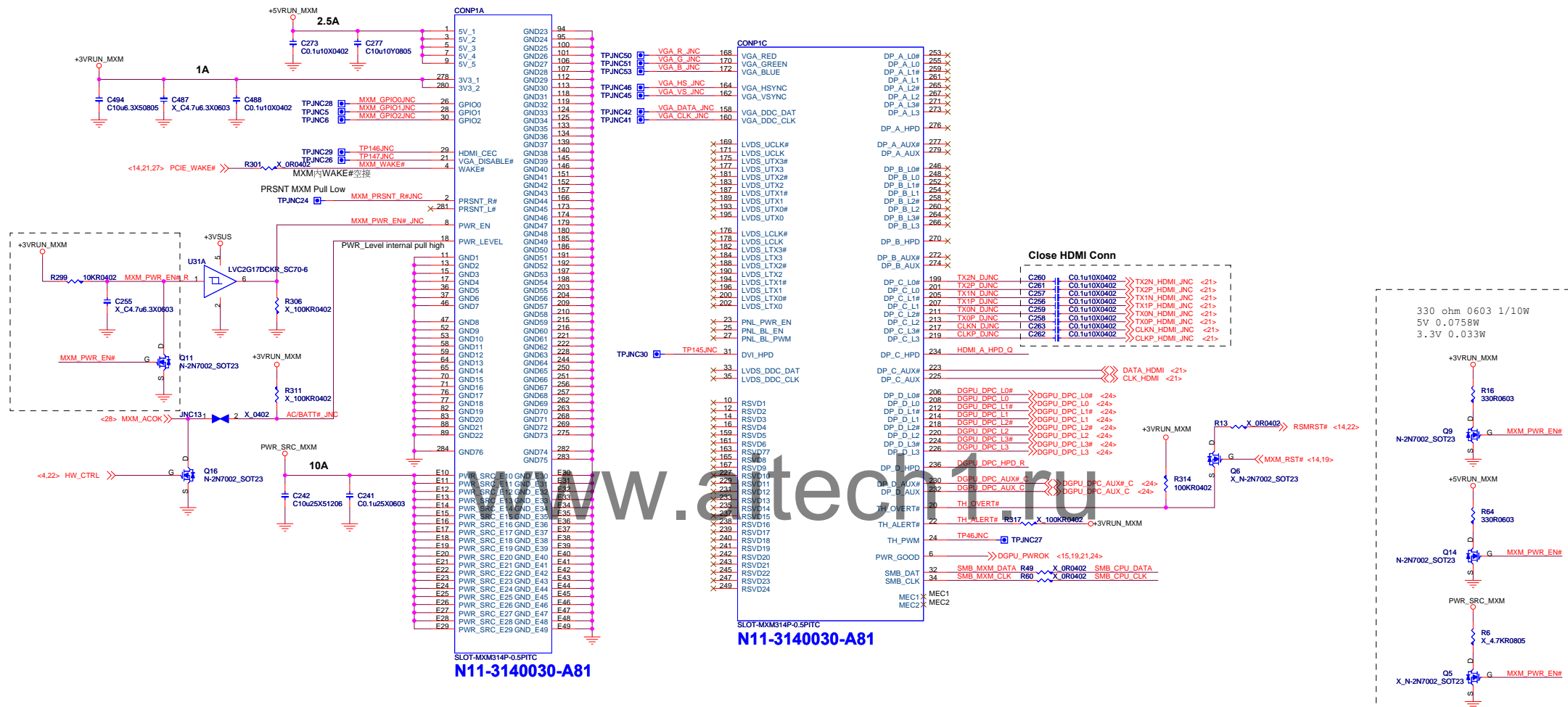


USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	
1	2	USB 3.0 Port 2	Debug Port
2	5	USB 3.0 Port 3	
3			NC
4		WebCam (LVDS)	
5		USB 2.0 Port 5 (1763)	
6			NC
7			NC
8		USB 2.0 Port 5 (1763)	
9		USB 2.0 Port 5 (16F4)	Debug Port
10		TestPad	
11		EPF LED (8051)	
12		Mini PCIE-BT	
13			NC
	3		NC
	4		NC
	6		NC

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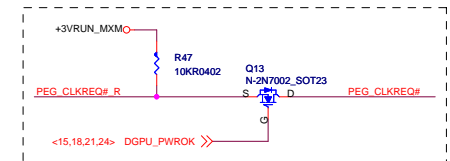
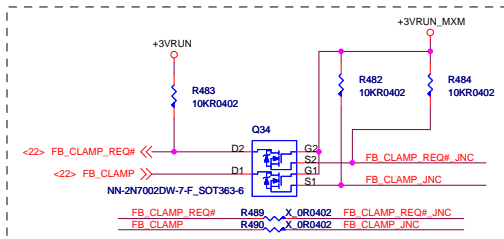
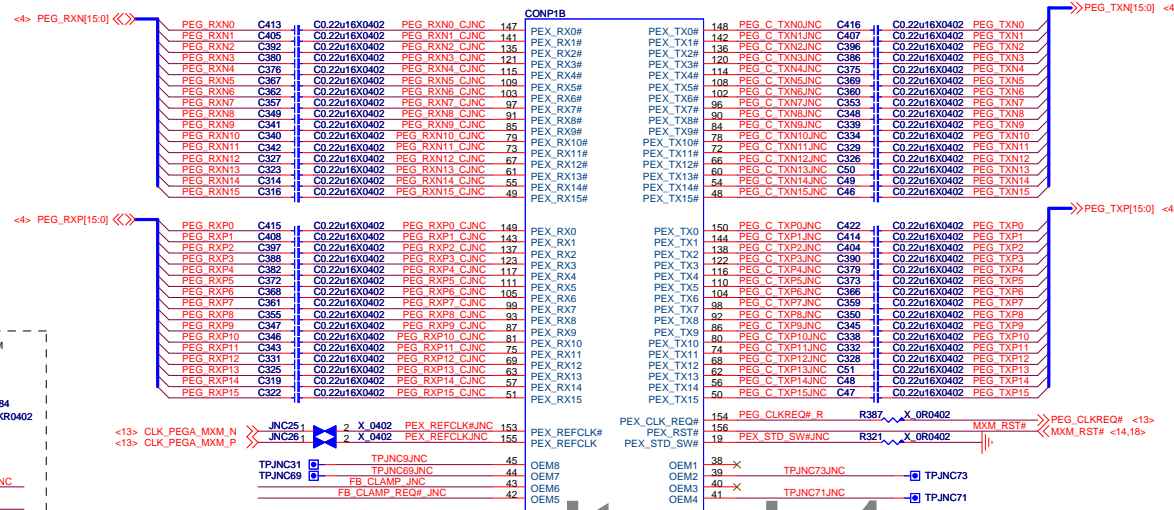
MXM 3.0 (x16 PEG Gen 3)



MXM 3.0 (x16 PEG Gen 3)

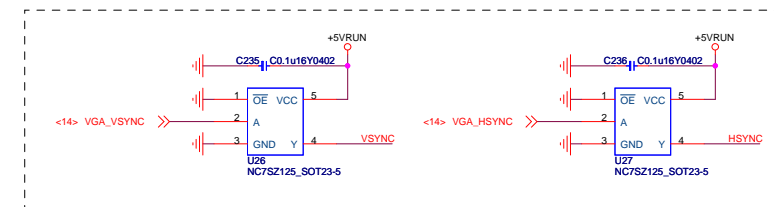
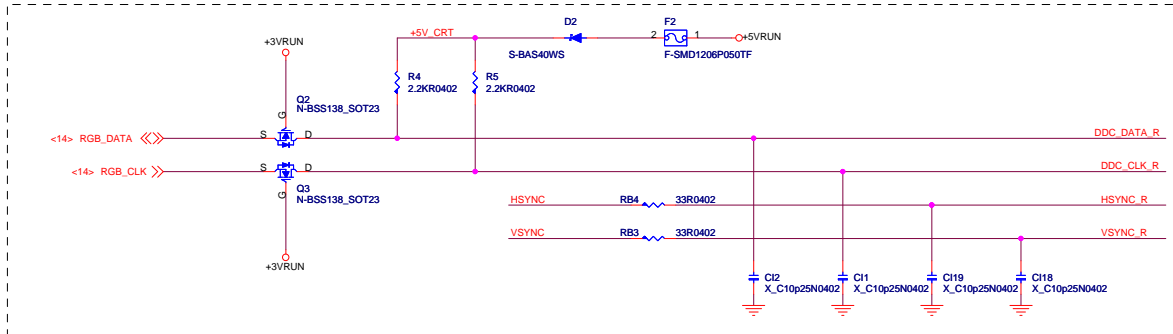
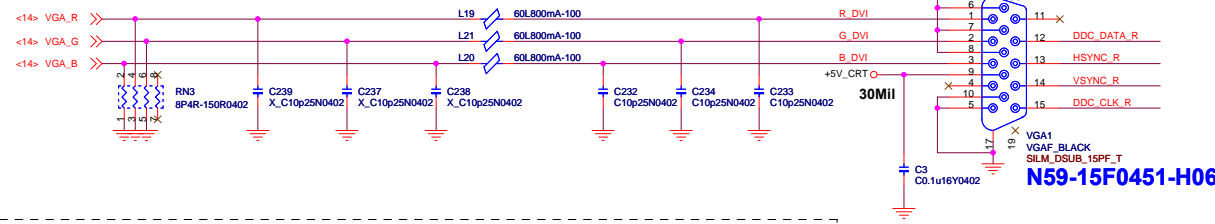
n'VIDIA Comments: NV11 can't support PCIe GEN3,so used 0.1uf CAP

The change in AC capacitor value from 0.1uf to 0.22uf is to enable compatibility with futrue platforms having PCIe GEN3(8GT/s)

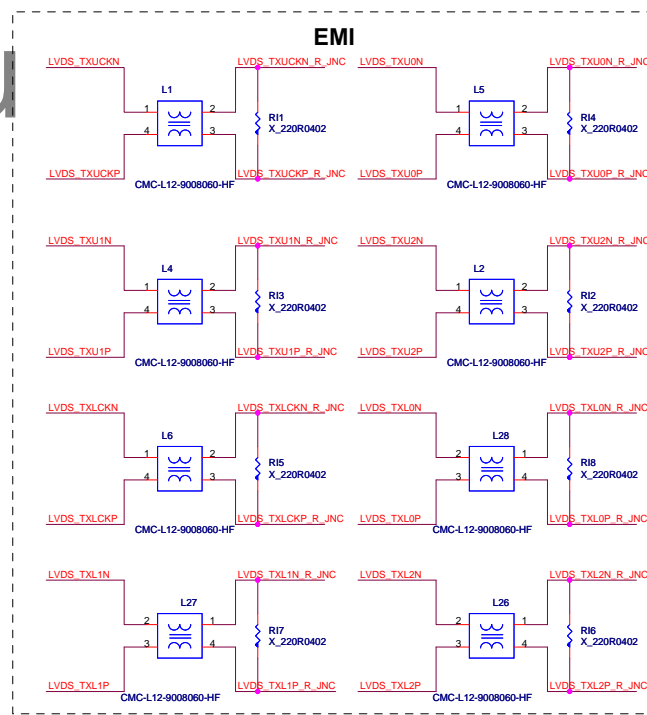
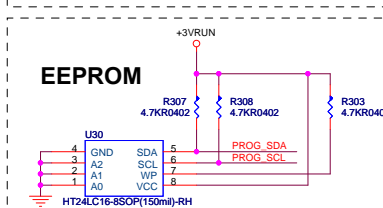
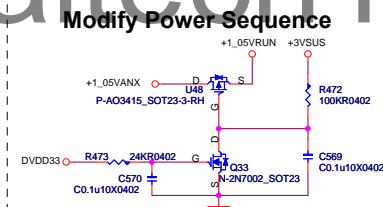
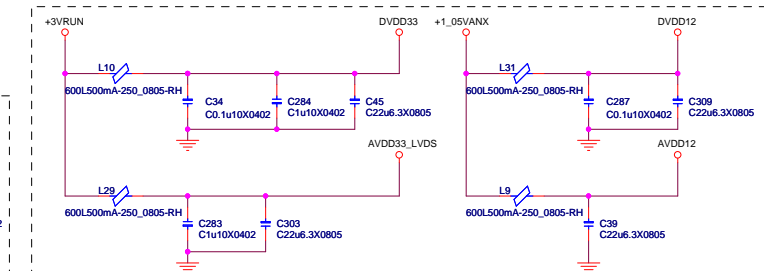
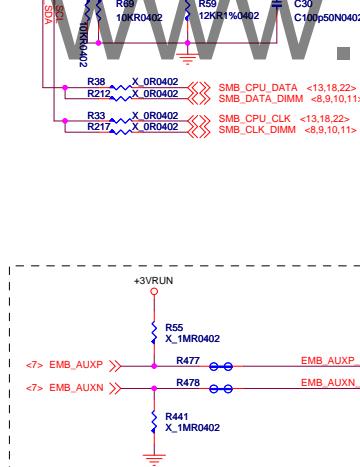
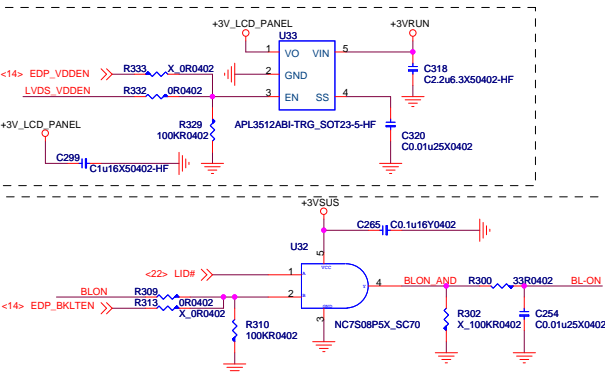
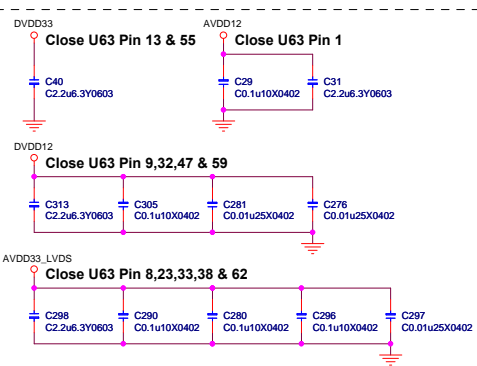
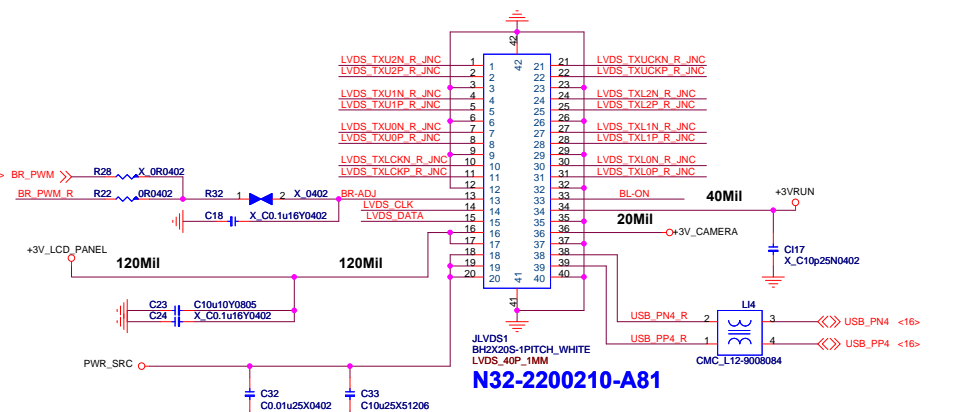
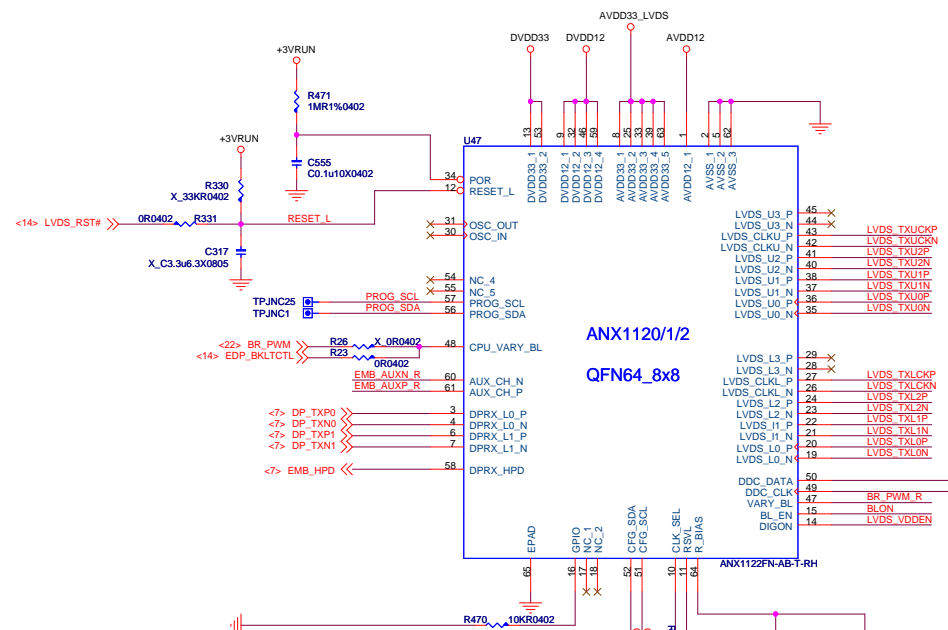


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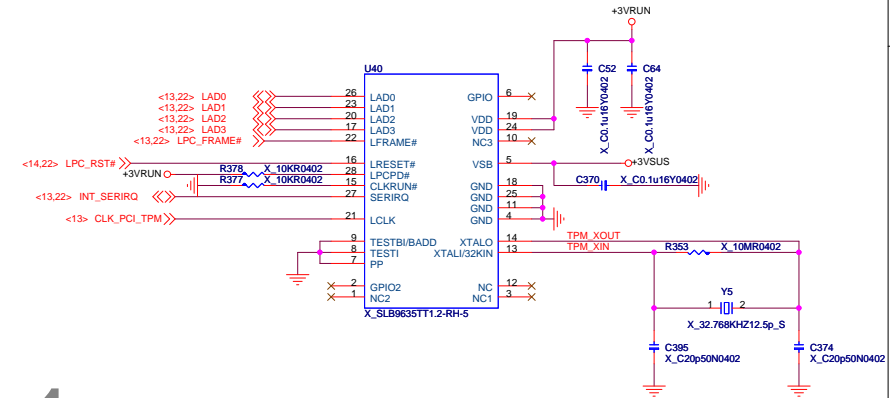
CRT



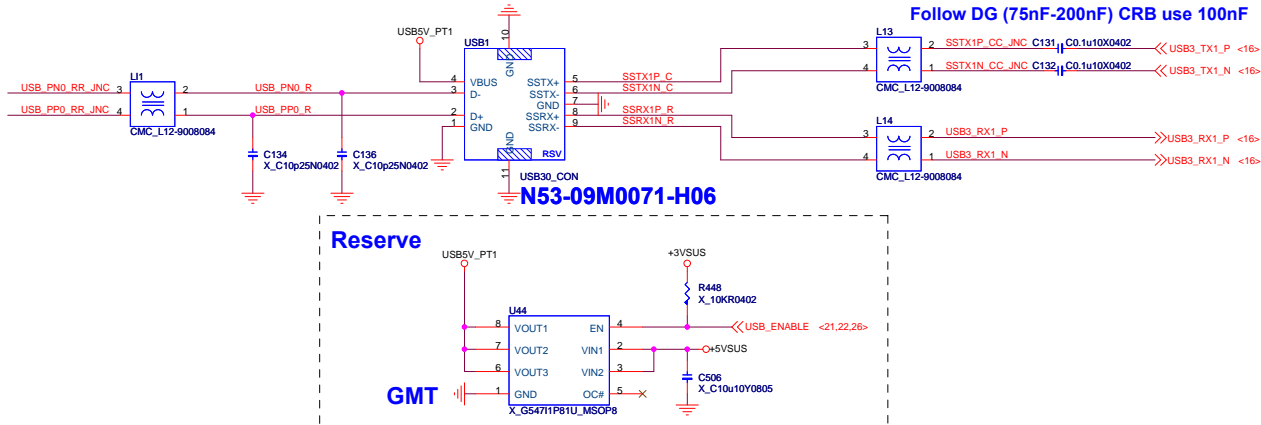
eDP to LVDS



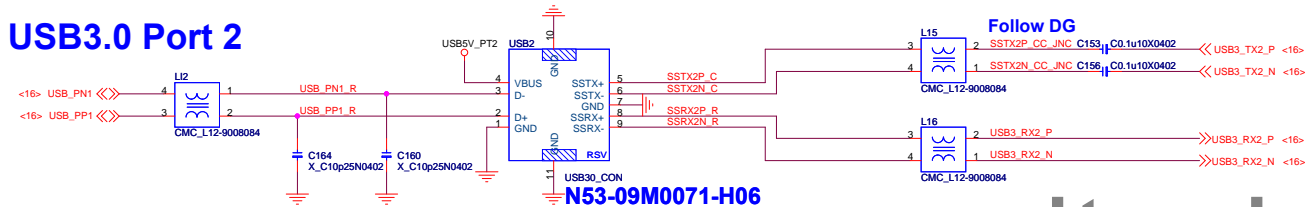
TPM



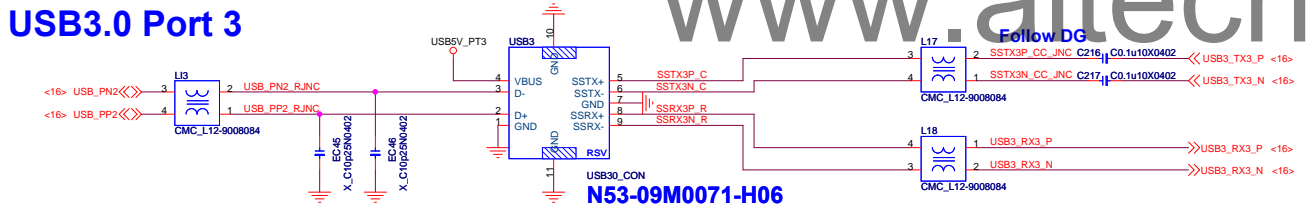
USB3.0 Port 1



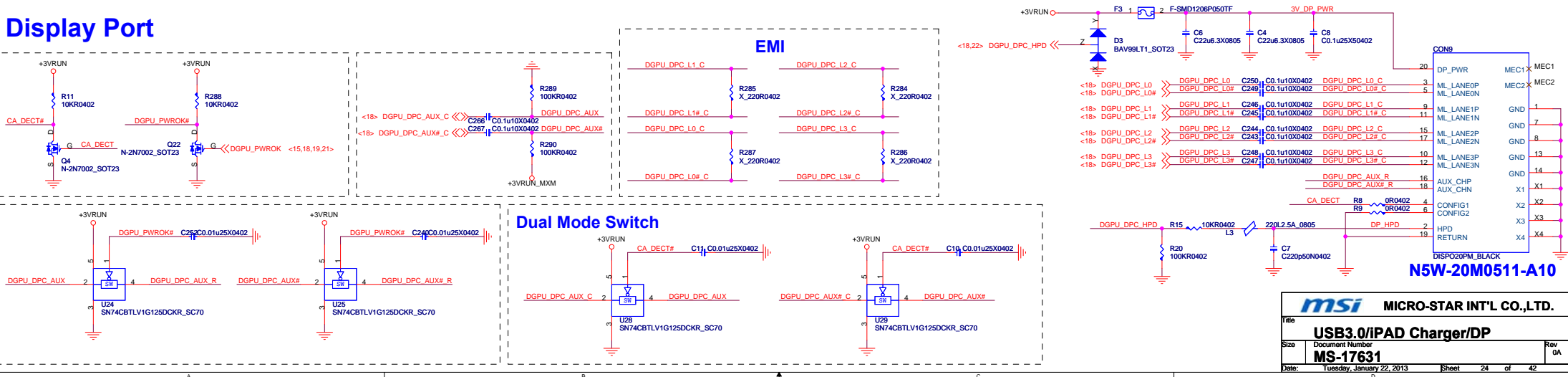
USB3.0 Port 2

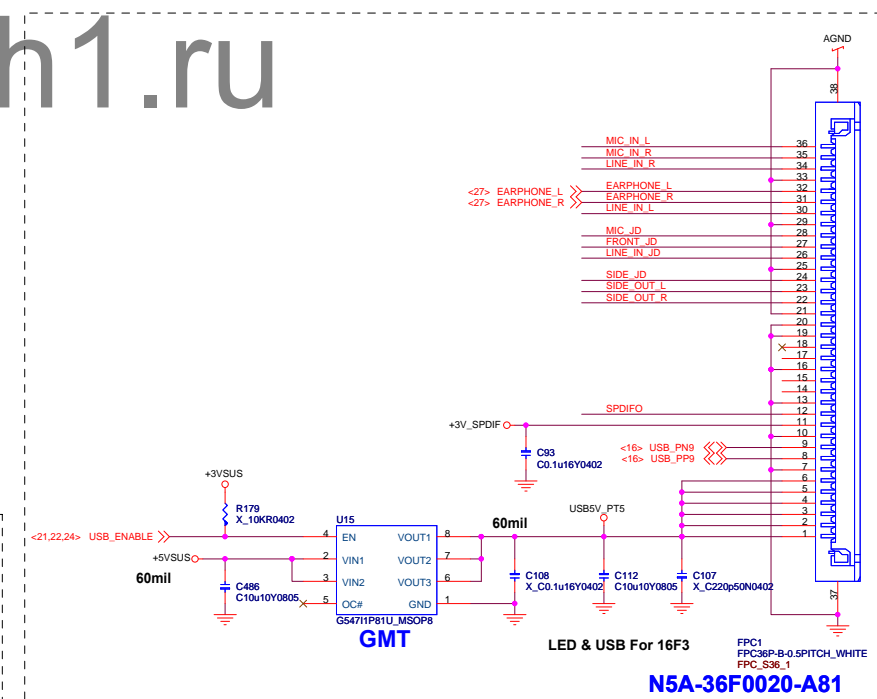
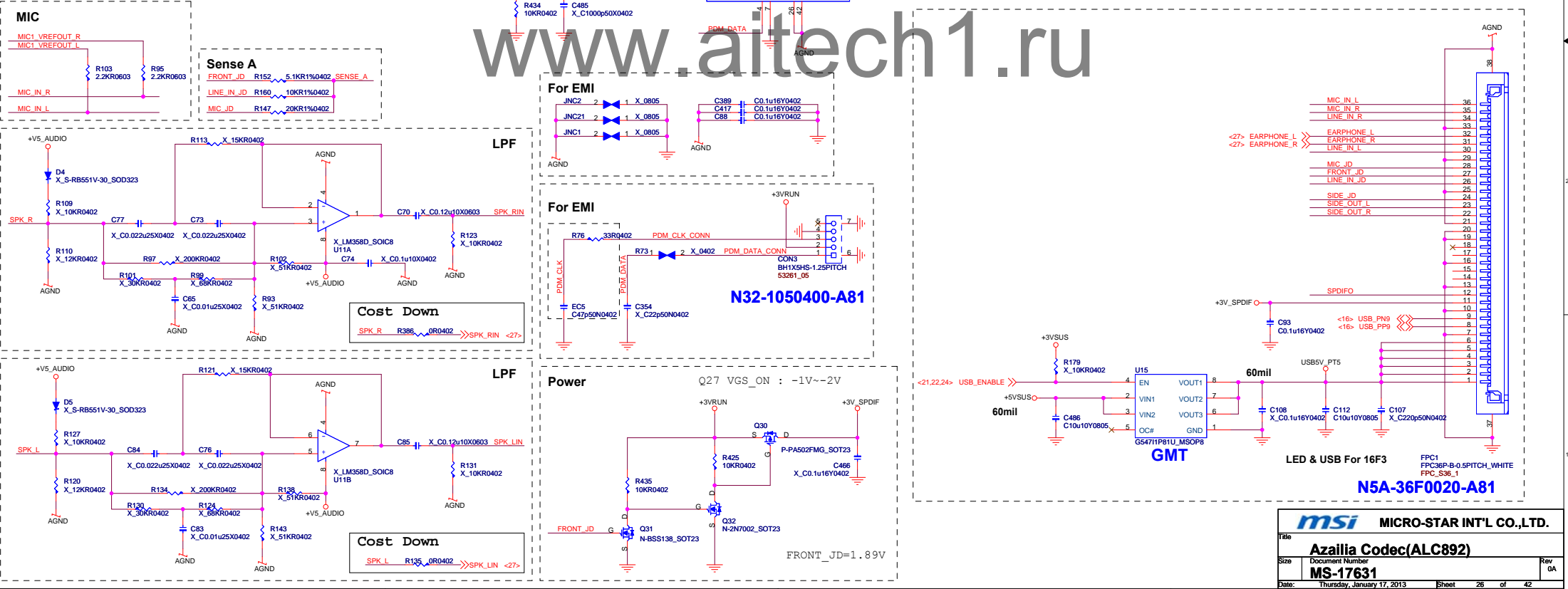


USB3.0 Port 3

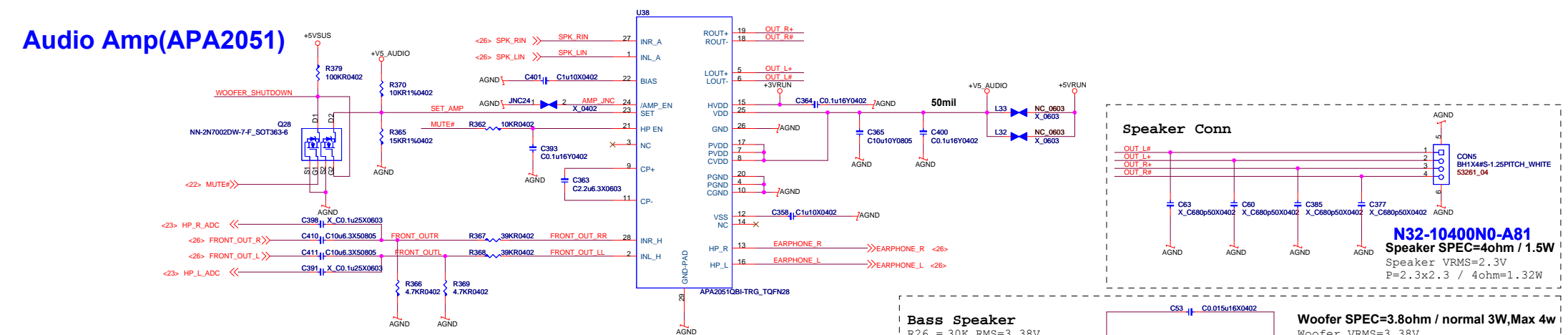


Display Port

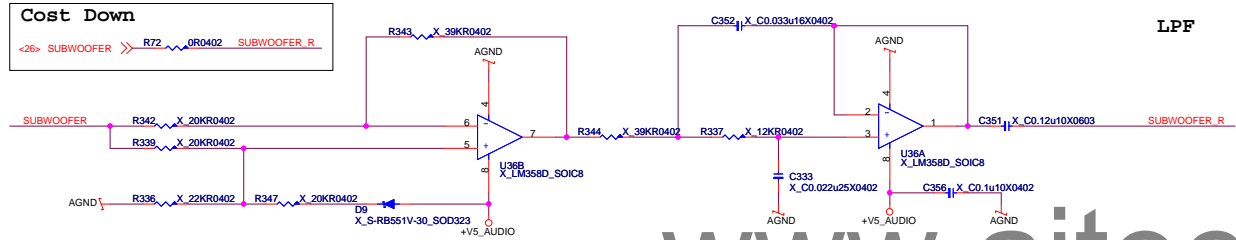




Audio Amp(APA2051)

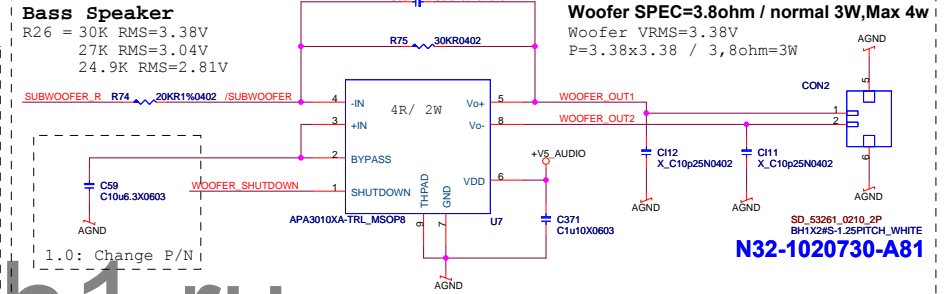


Cost Down

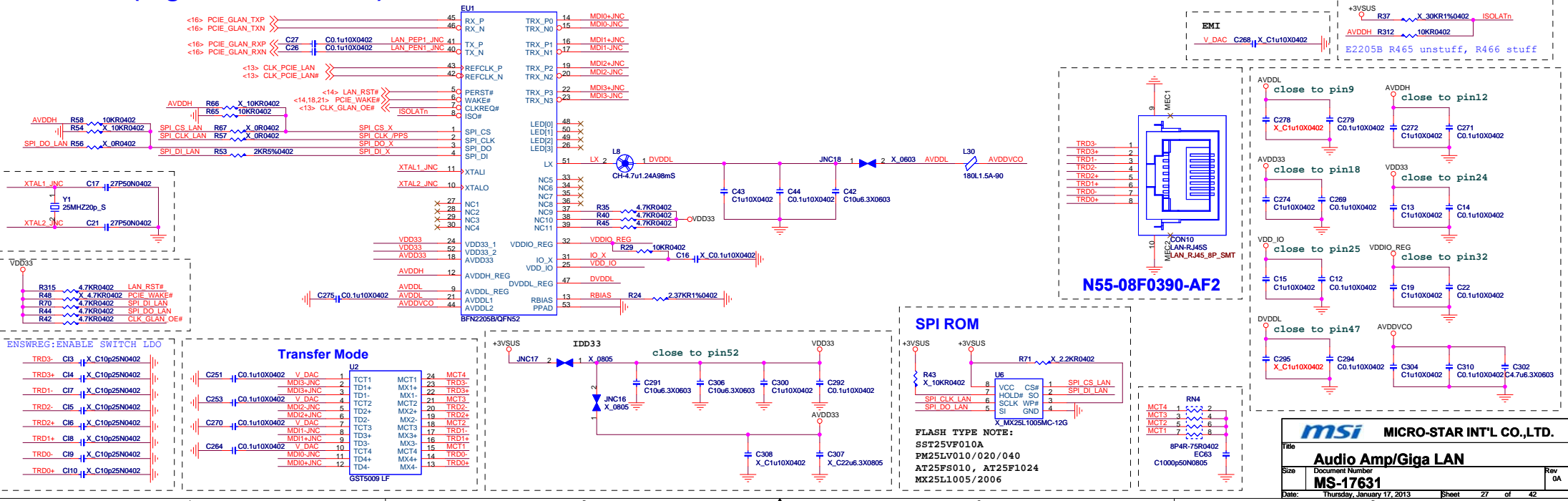


| Bass Speaker

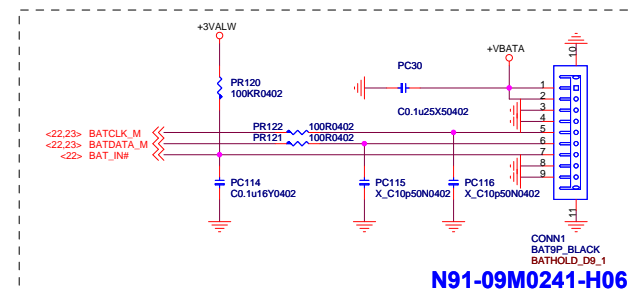
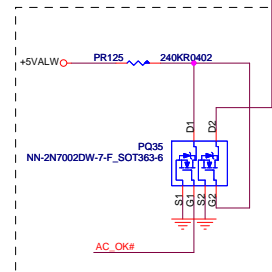
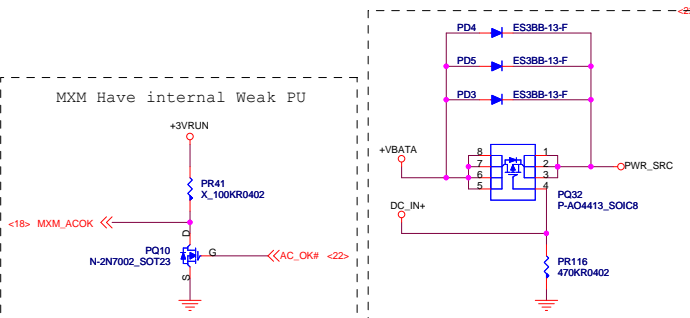
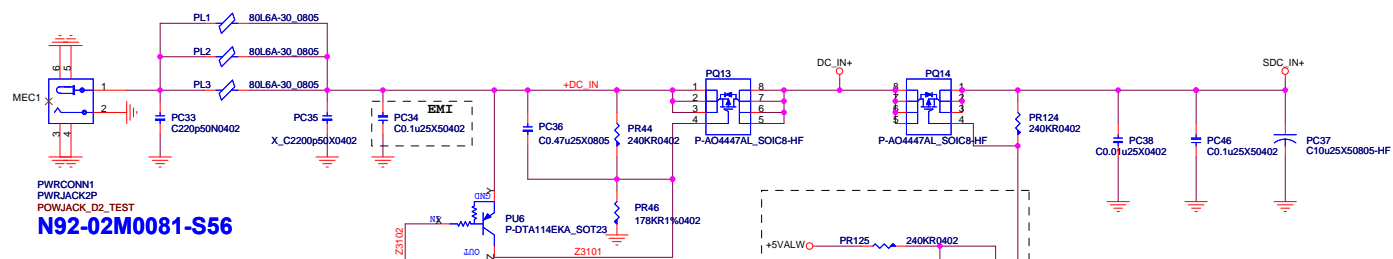
```
R26 = 30K RMS=3.38V
      27K RMS=3.04V
      24.9K RMS=2.81V
```



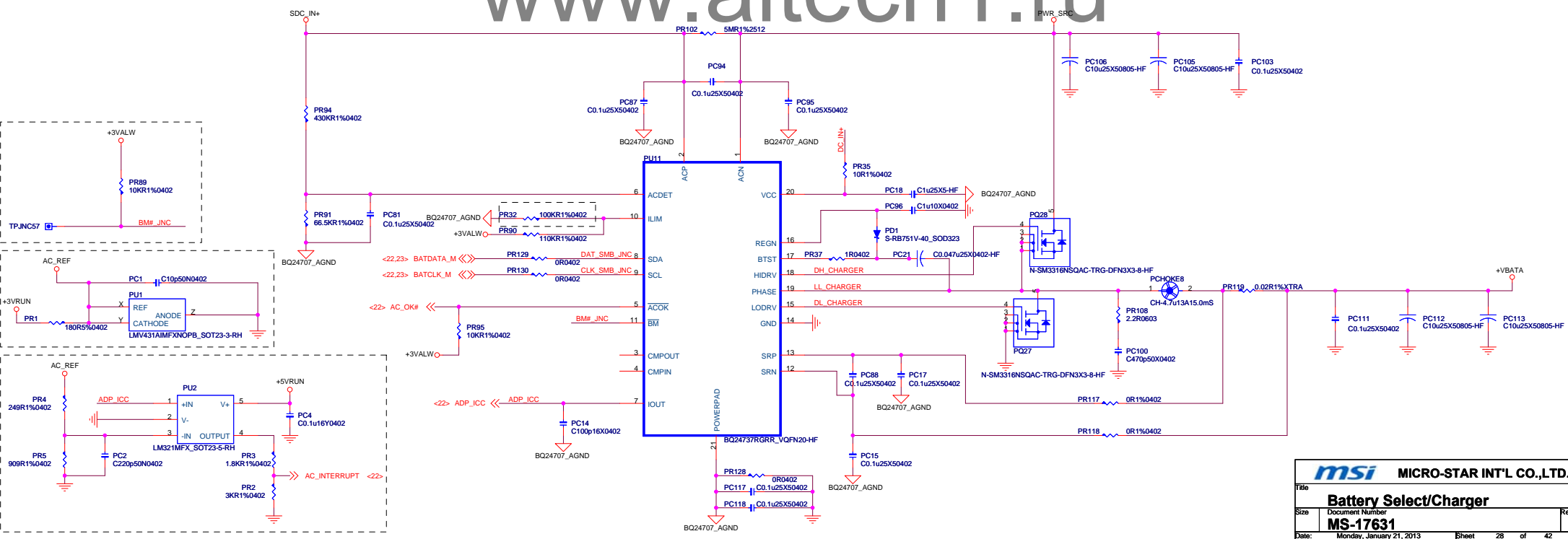
GIGA LAN(Big Foot BFN2200B)



Battery Select



Battery Charger

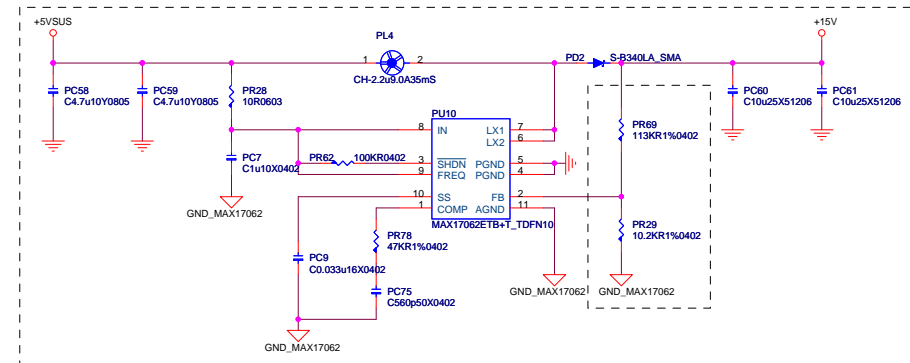
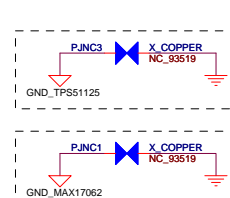
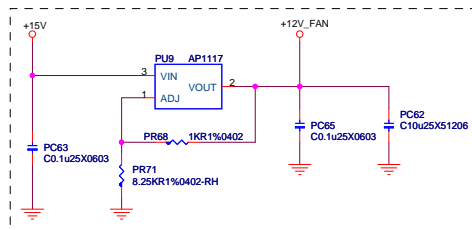
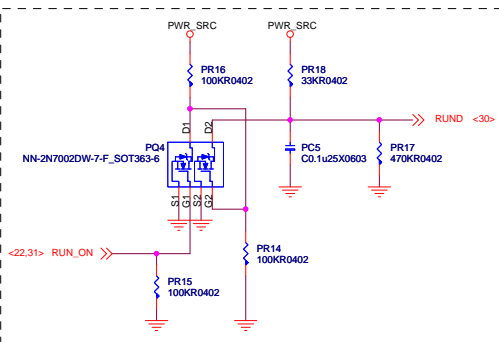


System Power (3V,5V)

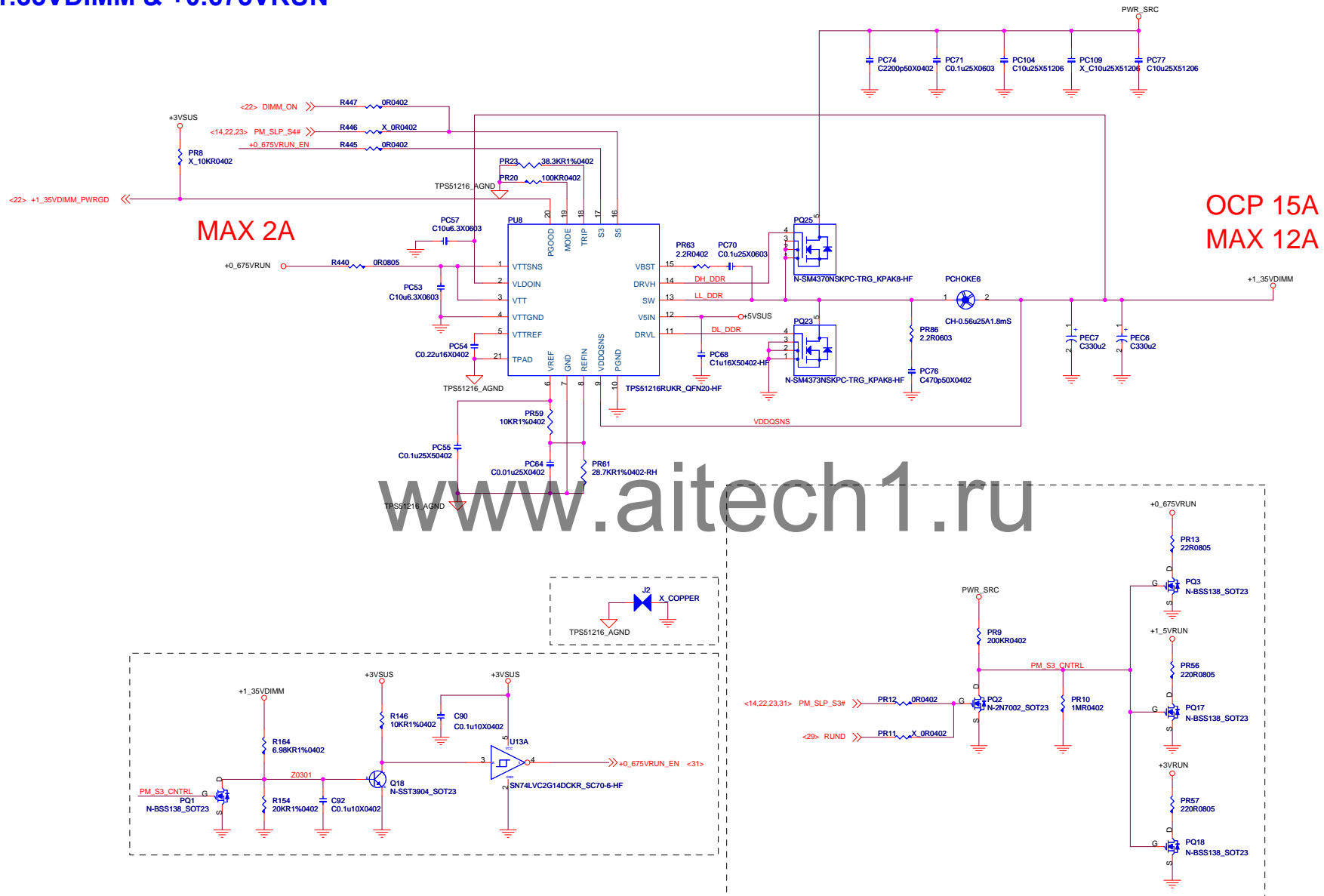
OCP 7A
MAX 6A

OCP 12A
MAX 10A

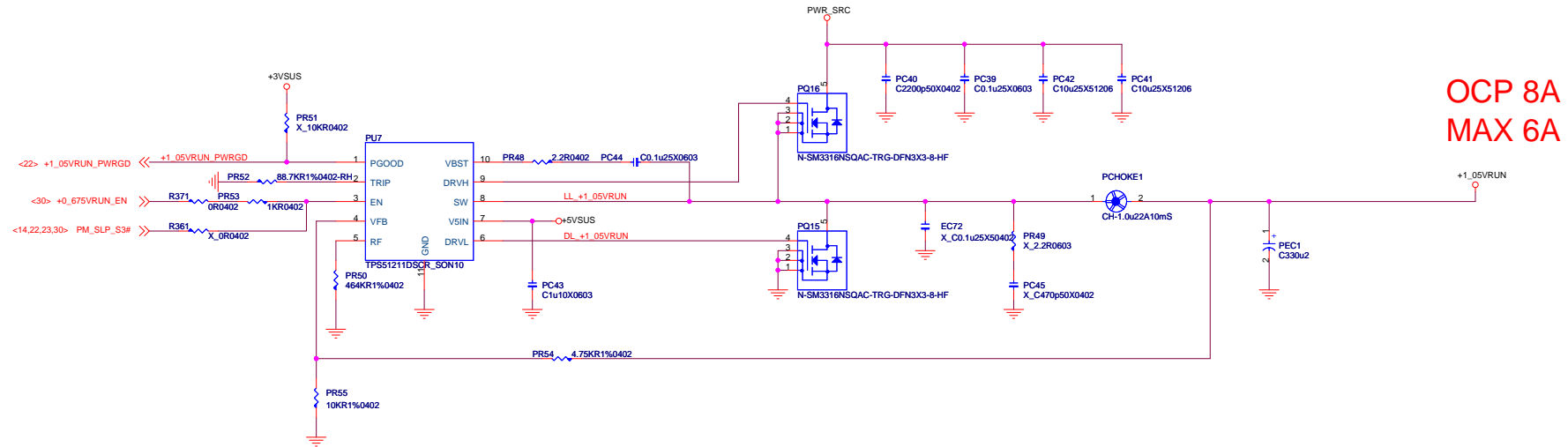
www.aitech1.ru



+1.35VDIMM & +0.675VRUN

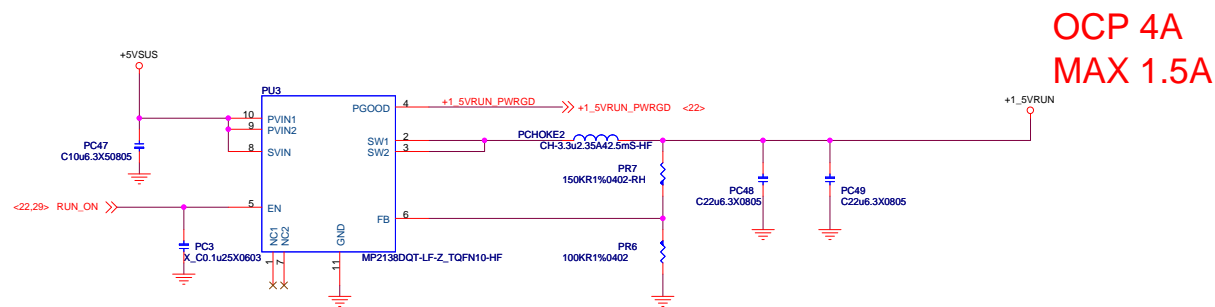


+1.05VRUN

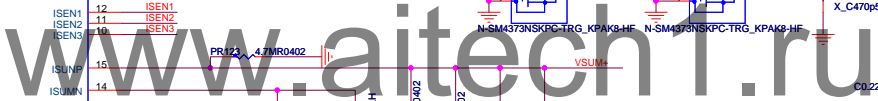


www.aitech1.ru

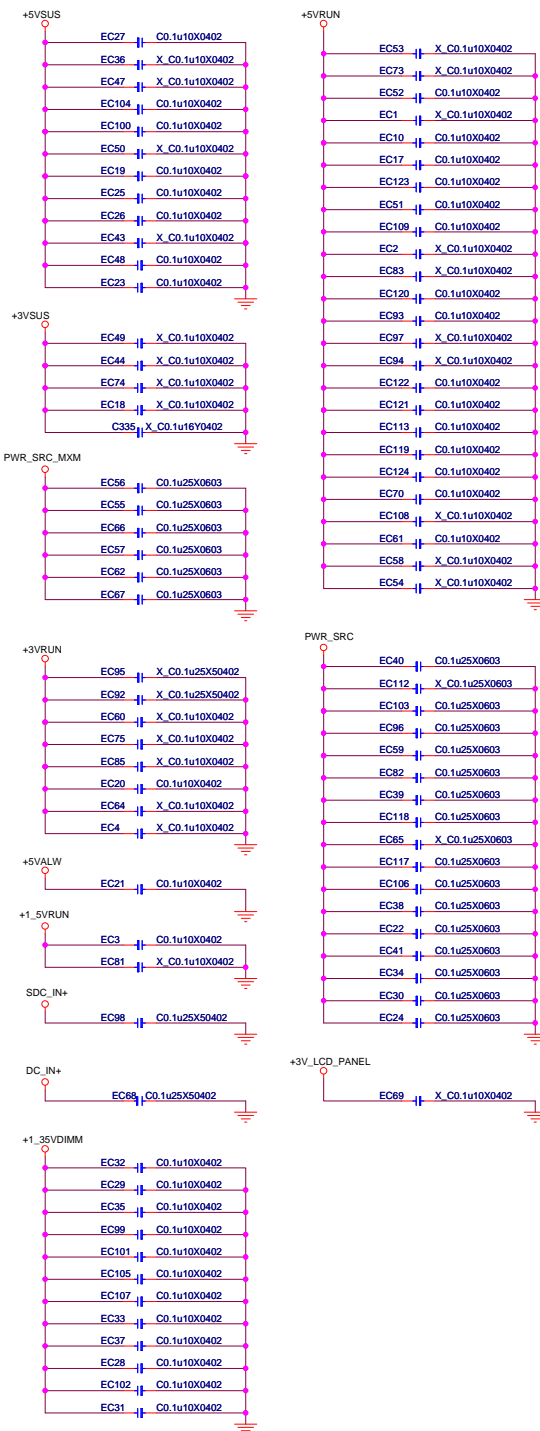
+1.5VRUN



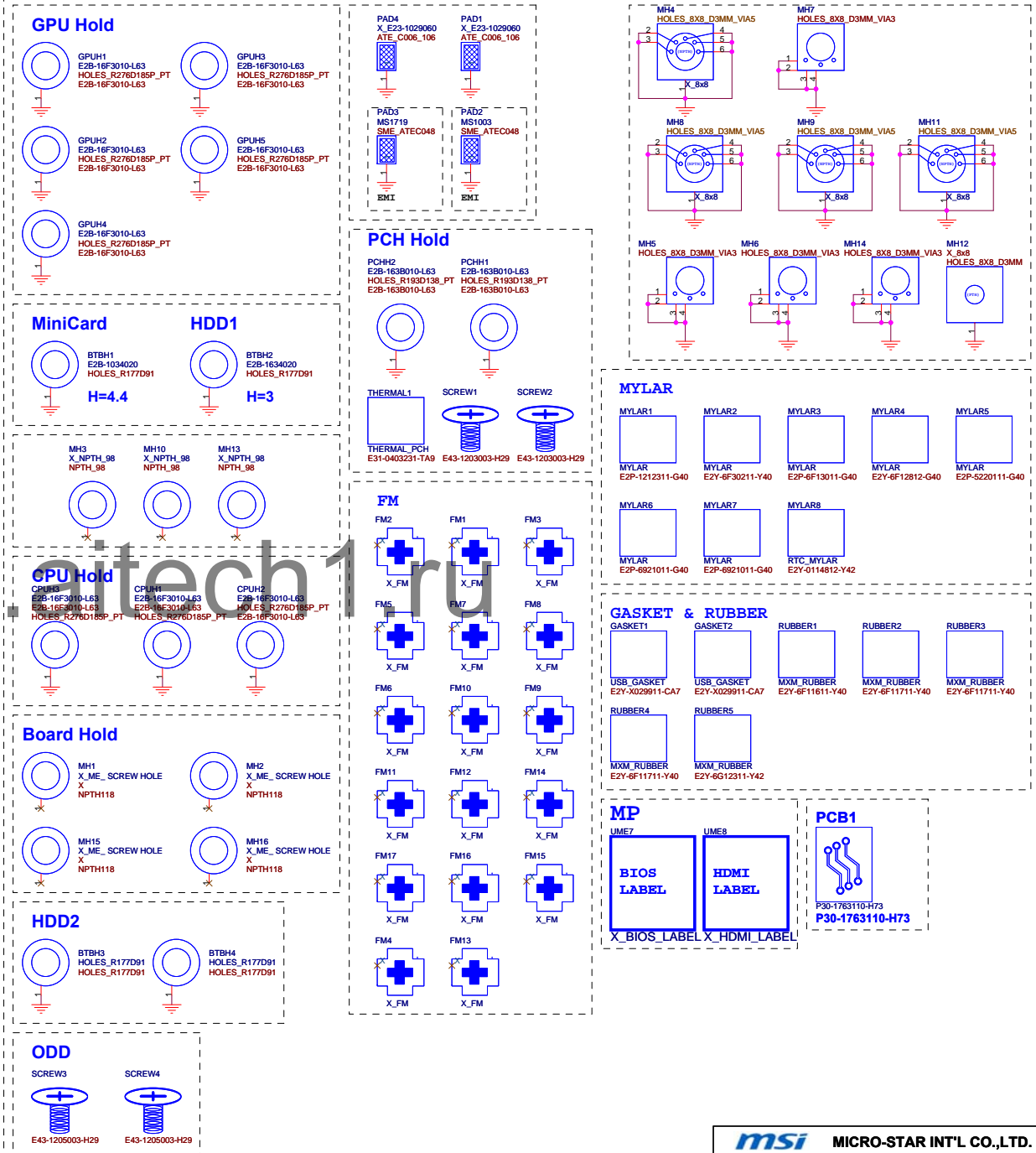
CPU Core Power(ISL95812HRZ)



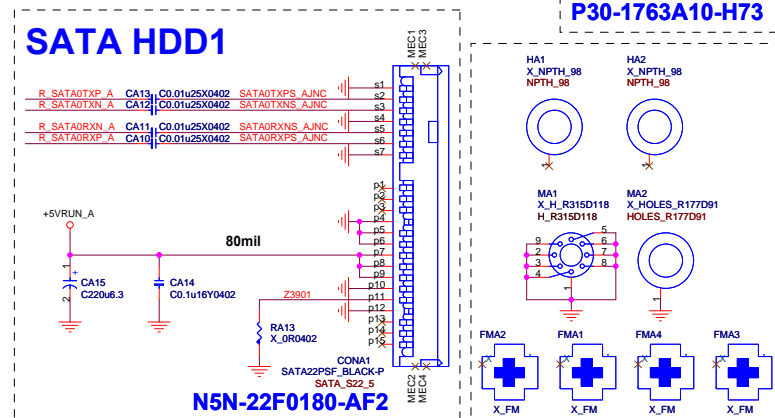
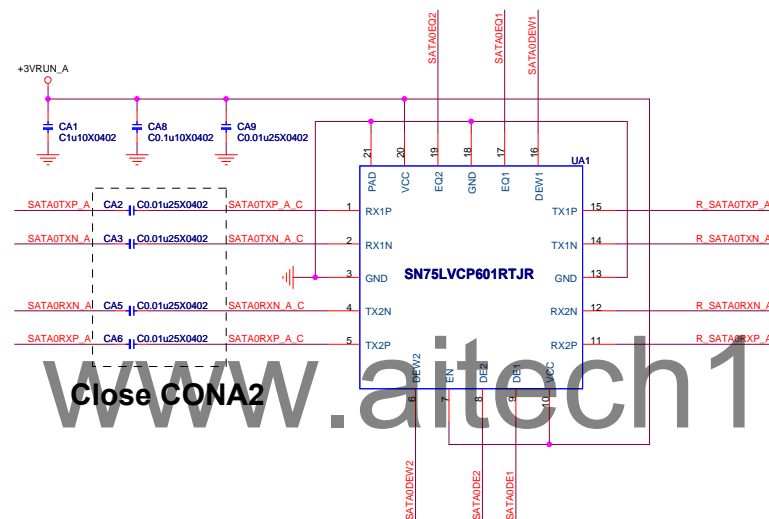
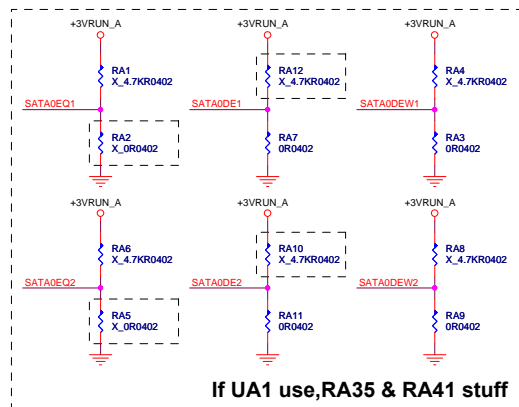
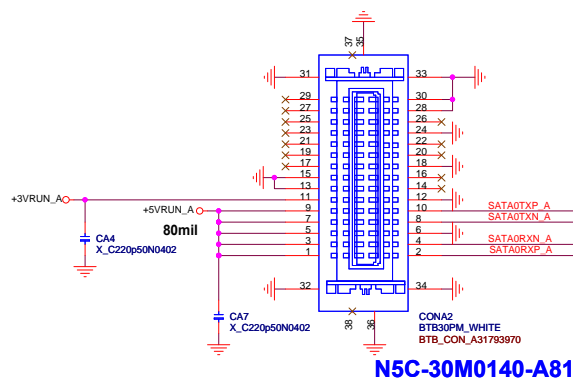
EMI



Screw



BTB Conn From Port 3



TI SN75LVCP601RTJR HW Setting

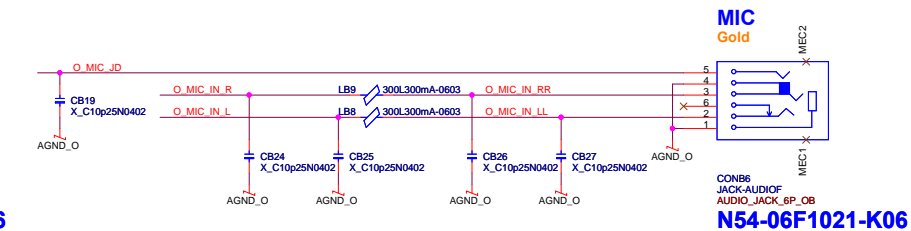
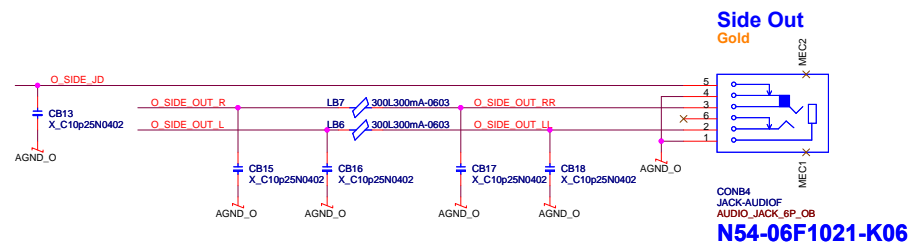
EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)	DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps)
NC (default)	0	NC (default)	-6
0	7	0	0
1	14	1	-3

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

MS-1763A Change List

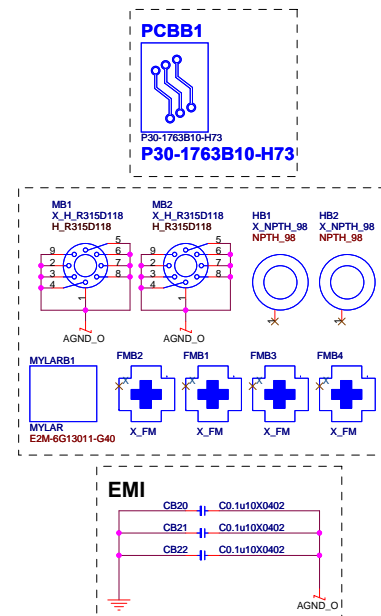
[illegible]

10

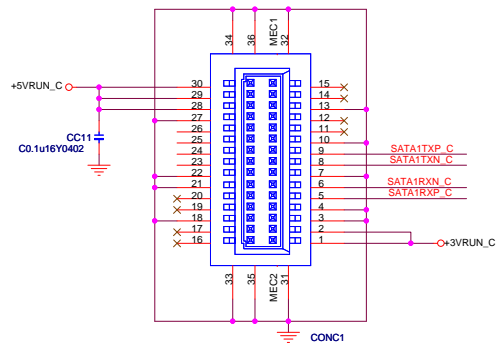


Date	Page	Description	Date	Page	Description
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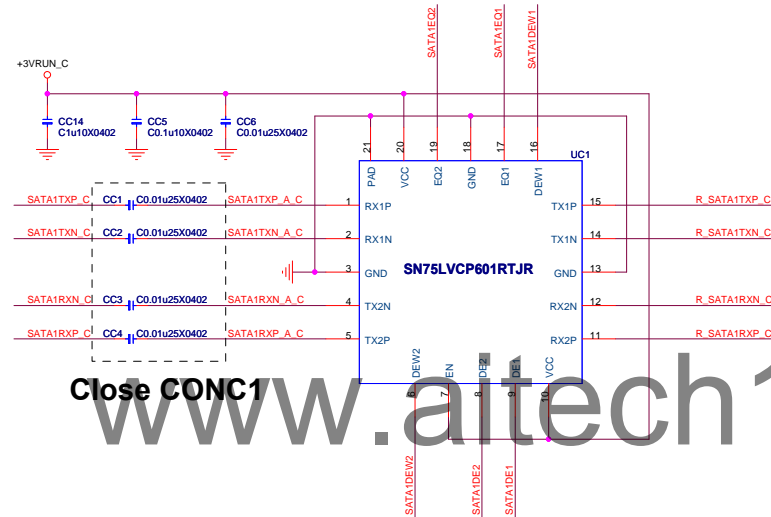
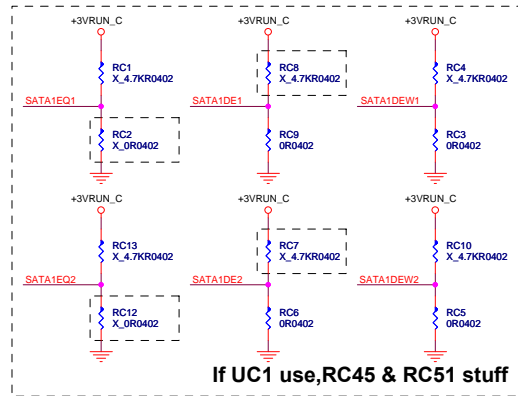
www.aitech1.ru



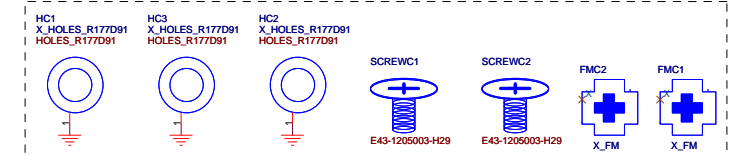
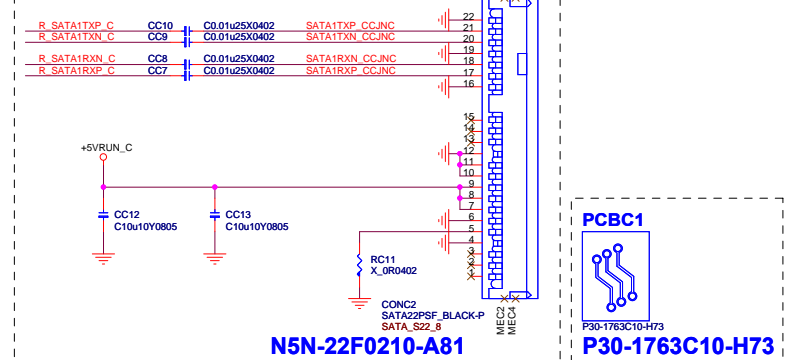
BTB Conn From Port 1



N5C-30M0170-A81



SATA Conn



TI SN75LVCP601RTJR HW Setting

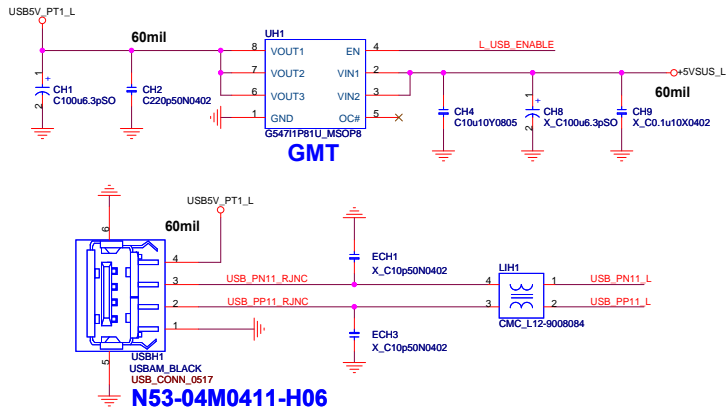
EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)	DE1/DE2	CH1/CH2De-Emphasis dB (@6Gbps)
NC (default)	0	NC (default)	-6
0	7	0	0
1	14	1	-3

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

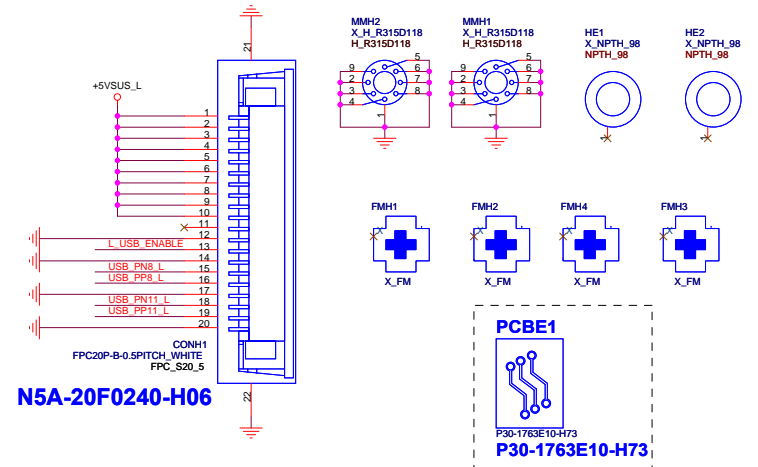
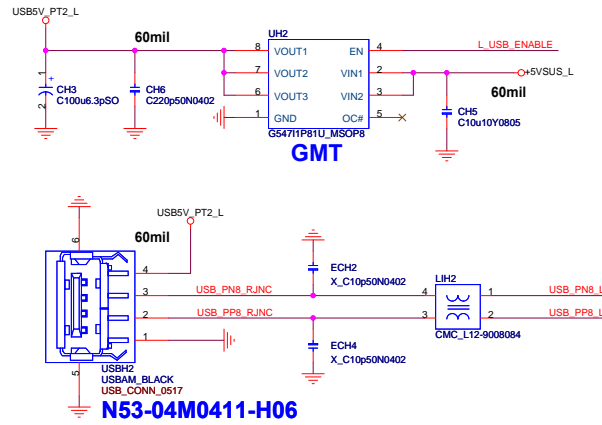
MS-1763C Change List

[illegible]

USB4



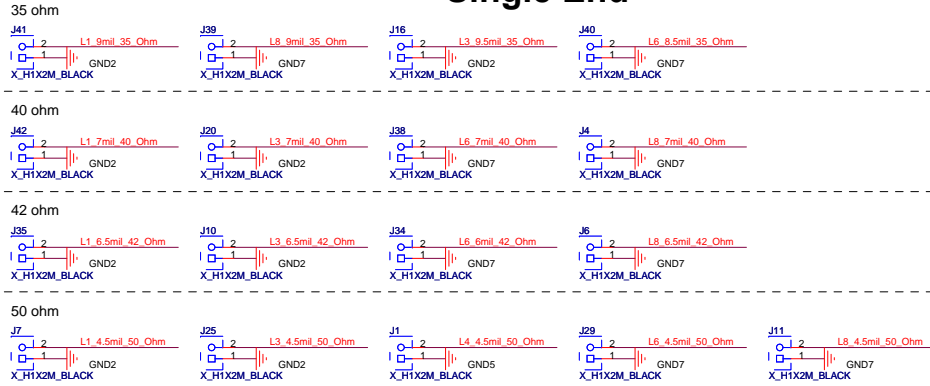
USB5



MS-1763E Change List

[illegible]

Impedance Single End

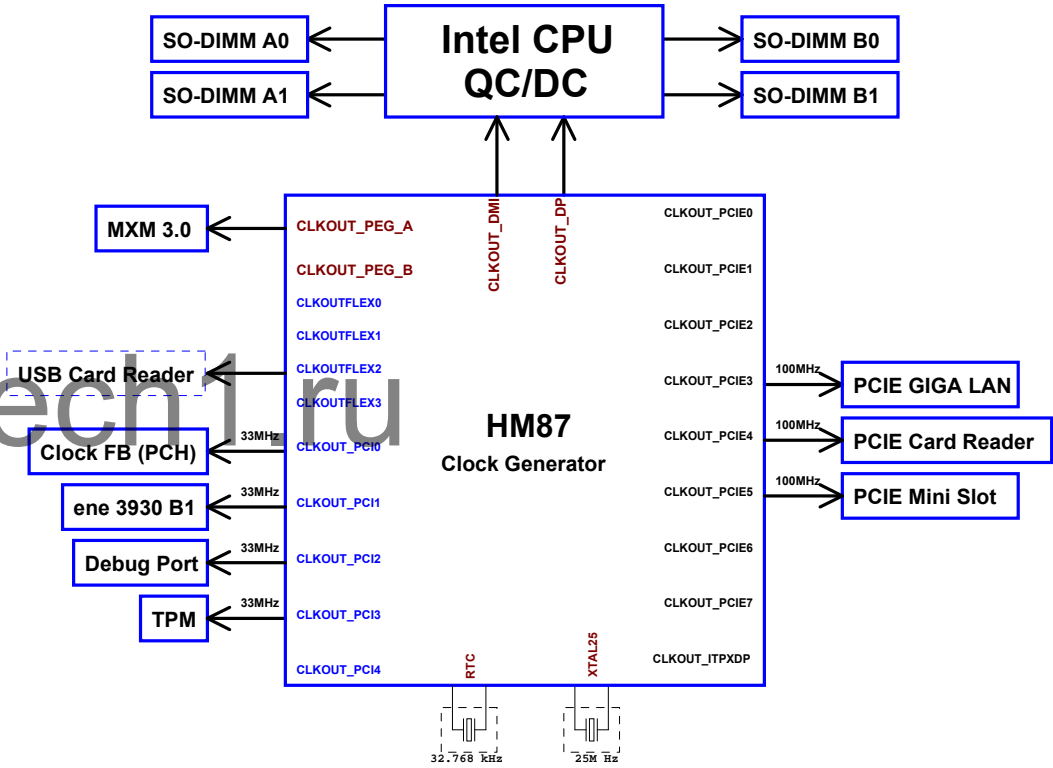


Differential



Clock Distribution

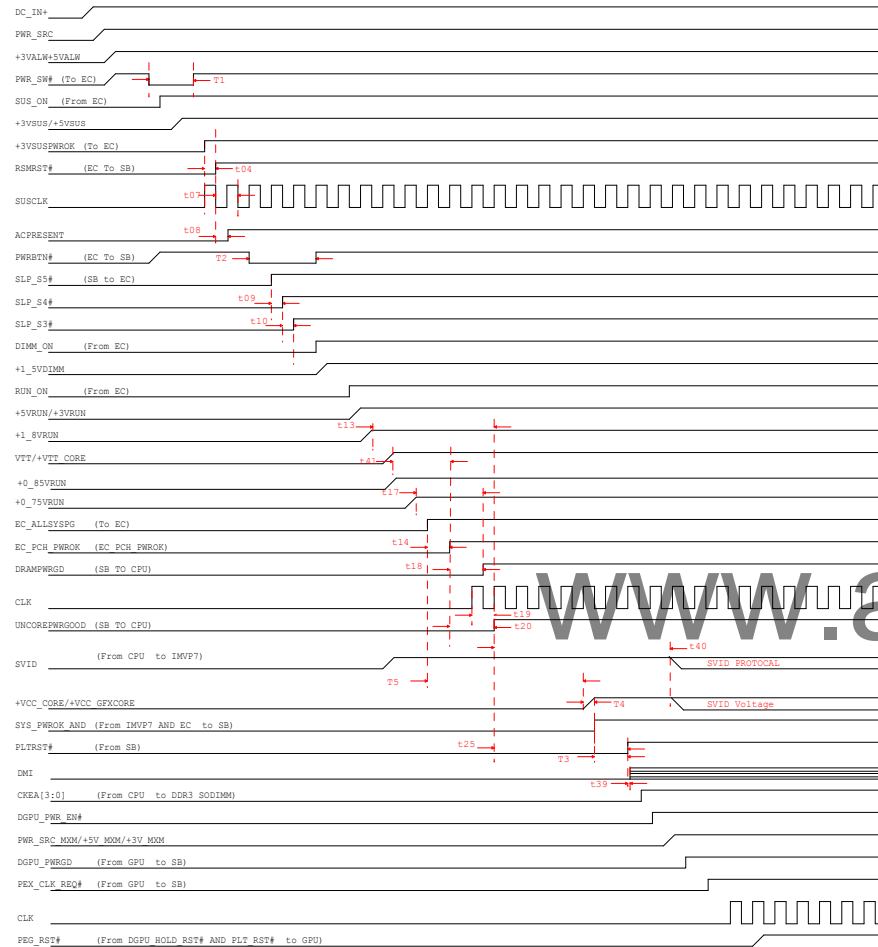
Internal Clock Mode



Power on Sequence

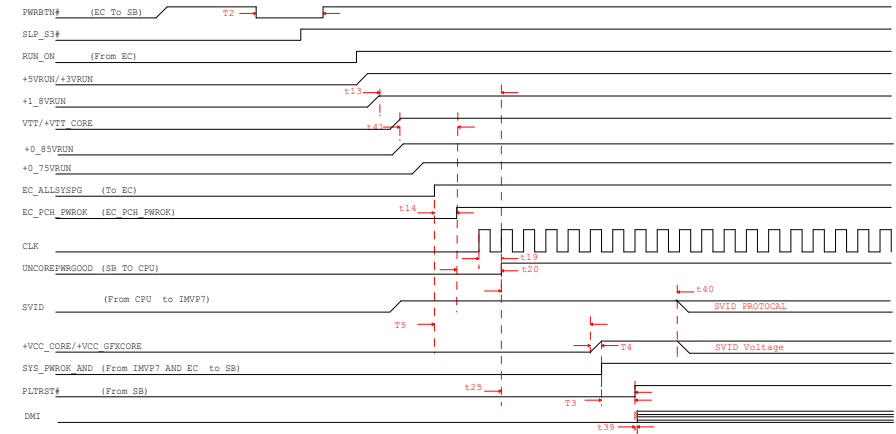
S5-S0

EC programming timing



S3-S0

EC programming timing



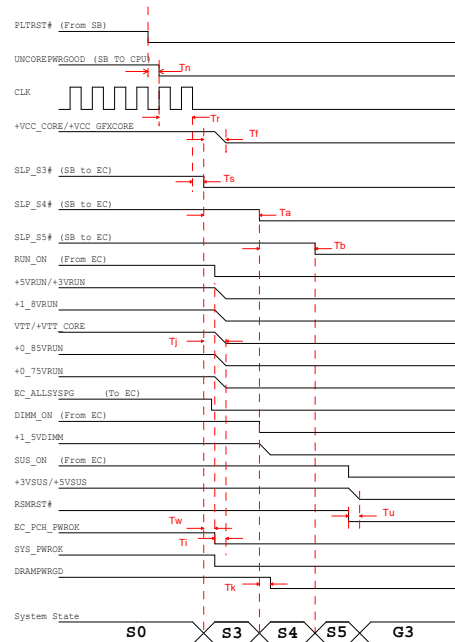
www.aitech1.ru

	Min	Max	Unit	Description
T1	150		ms	
T2	16		ms	
T3	1		ms	Timing set by PCH
t04	10		ms	
t07	100		ms	
t08		90	ms	
t09	30		us	
t10	30		us	
t13	5	650	ms	
t14	99		ms	EC Delay
t17	2	650	ms	
t18	1		ms	Timing set by PCH
t19	41		ms	Timing set by PCH
t20	2		ms	Timing set by PCH
t25	1	100	ms	
T5		800	us	Follow MVP Spec
T4	2.5		mV/us	Follow MVP Spec
t39		200	us	
t40		500	us	
t41	10		ms	

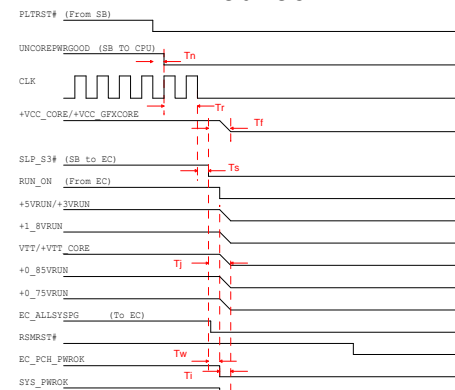
Power down Sequence

S0-S5

EC programming timing

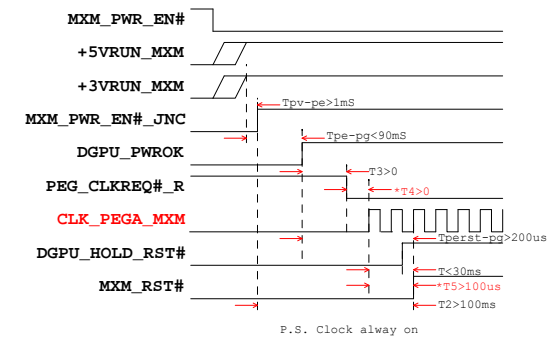


S0-S3

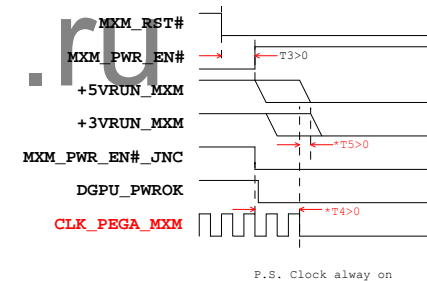


	Min	Max	Unit	Description
Ta	30		uS	
Tb	30		uS	
Tf		500	mS	
Ti	40		nS	
Tj	5		uS	
Tk	100		nS	
Tn	30		uS	
Tp	500		uS	Sx-RSMRST#
Tr	10		uS	
Ts	1		uS	
Tu	40		nS	
Tw	0		mS	

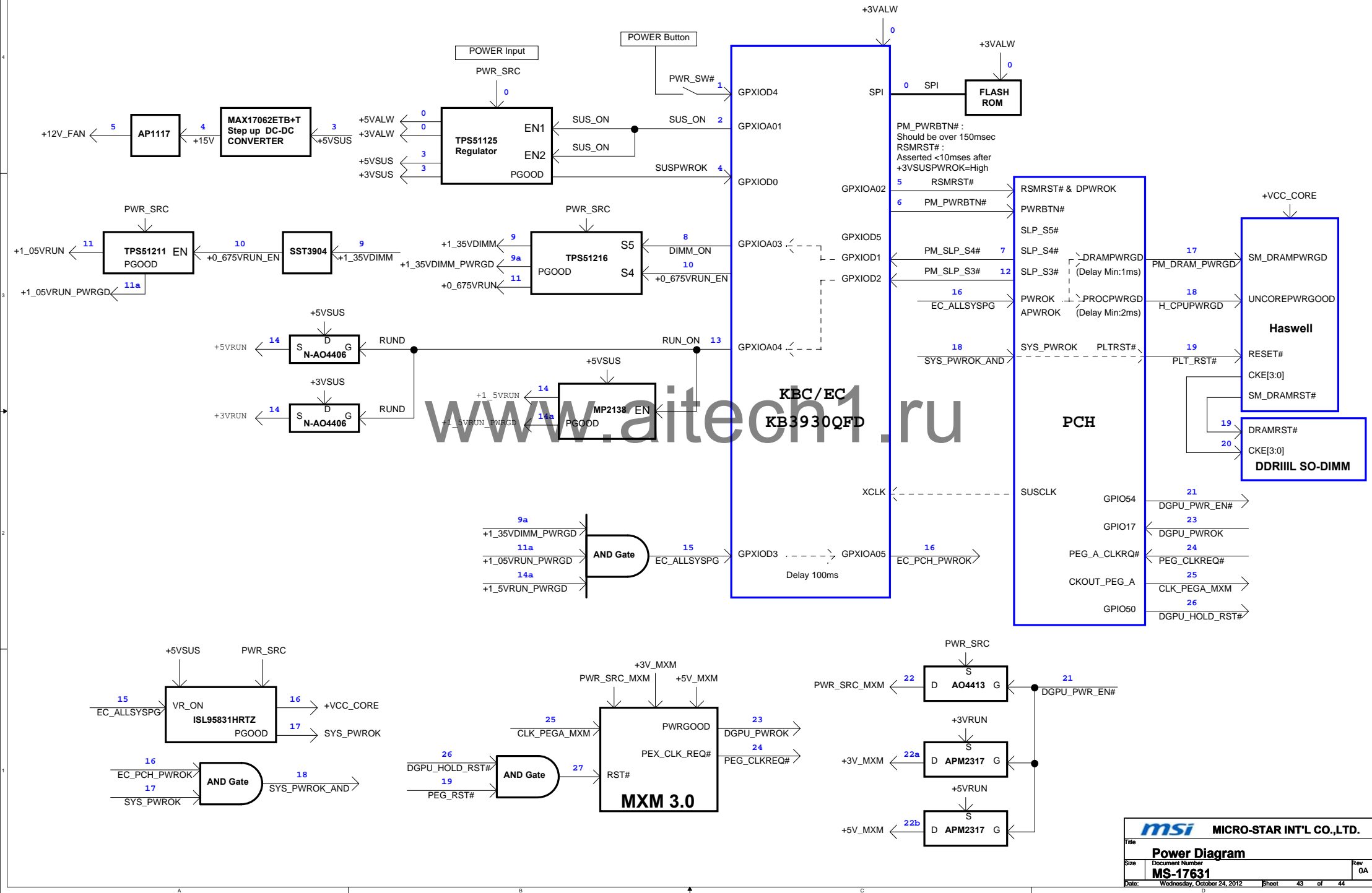
Power-Up Sequence For Optimus On MXM



Power-Down Sequence For Optimus On MXM



Power Diagram



DC_IN
Adaptor 180W

BQ24737
Charger

ISL95812HRZ
+VCC_CORE

N MOS
SM4370N

N MOS
SM4373N

+VCC_CORE / 85A

TPS51216RUKR
+1_35VDIMM

N MOS
SM4370N

N MOS
SM4373N

+1.35VDIMM / 16.2A

+0.675VRUN / 2A

TPS51211DSCR
+1.05V

N MOS
SM3316N

N MOS
SM3316N

+1.05VRUN / 6.68A

TPS51125RGER
+3VALW/+5VALW

N MOS
SI4914BDY

N MOS
SM4370N

N MOS
SM4373N

+3VSUS / 9.586A

N MOS
AO4406AL

+3VRUN / 7.733A

N MOS
AO4406AL

+5VRUN / 6.5A

MAX17062ETB+T
+15V

AP1117
+12V

+15V / 2.16A

+12V / 2.7A

MP2138DQT
+1.5VRUN

+1.5VRUN / 624mA

KB3930QFB1
VCC 3.3VALW 20mA

MXM 3.1	
PWR_SRC	19V 10A
3.3V	3VRUN 1A
5V	5VRUN 2.5A

ANX1122	
3.3V	3VRUN 0.081mA
1.05V	1.05VRUN 0.11mA

TPM	
VSB	3VSUS 25mA
VDD	3VRUN 5mA

Camera	
VCC	3VRUN 350mA

MCU	
VCC	3VRUN 25mA

P2501	
VCC	3VRUN 25mA

Haswell (rPGA 947)	
VCC_CORE	1.2V 85A
VDDQ	1.35V 4.2A
Lynx Point HM87	
VCC3_3	3.3V 223mA
VCCIO	1.05V 6.67A
VCCVRM	1.5V 179mA
VCCDSW	3.3V 286mA
VCCADAC	1.5V 70mA
DDR 3L	
VDDQ	1.35VDIMM 12A
VREF	0.675VRUN 2A
LVDS	
VDD	3.3VRUN 2A
VLED	19V 1.5A
Realtek RTS5209	
3V3_IN	3VRUN 300mA
CPU FAN	
VCC	12V 2.7A
ALC892-CG	
VDD33	3VSUS 1mA
AVDD	5VSUS 60mA
DVDD	3VSUS 41mA
Amplifier	
VDD	5VSUS 485mA
HVDD	3VRUN 5mA
Mini PCI-E	
+3.3V	3VRUN 1.1A
+1.5V	1.5VRUN 375mA
USB Ports	
USB 2.0*2	5VSUS 1.5A
USB 3.0*3	5VSUS 6A
Bigfoot E2200	
VDD33	3VSUS 1.5A
SATA Ports	
HDD	5VRUN 2A
ODD	5VRUN 2A
mSATA	3VRUN 2.7A

Power Name	Current
VCC_CORE	85A
1.35VDIMM	16.2A
0.675VRUN	2A
1.05VRUN	6.68A
3VSUS	6.886A
3VRUN	5.033A

Power Name	Current
5VSUS	21.22A
5VRUN	6.5A
15V	2.16A
12V	2.7A
1.5VRUN	624mA
3VALW	20mA